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Intel® 815E Scalable Performance Board

Development Kit Manual

April 2001

Order Number: 273432-003

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Revision History

Revision	Date	Description
003	4/01	Kits upgraded to ship with 850 MHz Celeron processor (replacing 566 MHz processor). Baseboard BOM format changes (NO part changes); key components BOM expanded to include all kit components (excluding documentation, mounting hardware, etc.).
002	1/01	minor corrections, typos fixed
001	10/00	First publication of this document.

About This Manual 1

This manual tells you how to set up and use the evaluation board and processor assembly included in your Intel® 815E Scalable Performance Board Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” — This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started”— Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” — This chapter provides information on the system design.

Chapter 4, “Hardware Reference” — This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” — This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Appendix A, “Bill of Materials” — This appendix contains the bill of materials for the evaluation board.

Appendix B, “Schematics” — This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.

Numbers

Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure

The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names

Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax). Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1. Related Documents

Document Title	Order Number
Pentium® III Processor for the PGA370 Socket at 500 MHz to 1.0B GHz datasheet	245264
Intel® Pentium® III Processor Specification Update	244453
Intel® Pentium® III Processor Thermal Design Guide	273325
Intel® Celeron™ Processor up to 850 MHz datasheet	243658
Intel® Celeron™ Processor Specification Update	243748
Intel® 815E Chipset Platform Design Guide	298234
Intel® 815 Series Chipsets: 82815 Graphics Memory Controller Hub (GMCH) Datasheet	290688
Intel® 82801BA I/O Controller Hub 2 (ICH2) Datasheet	290687
Intel® 82802AB/82802AC Firmware Hub (FWH)	290658
Intel® 82802 Firmware Hub: Random Number Generator - Programmer's Reference Manual	298029
Intel® 815 Chipset: Graphics Controller Programmer's Reference Manual	298237
P6 Family of Processors Hardware Developer's Manual	244001
Intel Architecture Software Developer's Manual, Volume1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference Manual	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel Processor Serial Number application note	245125

Getting Started 2

This chapter identifies the evaluation kit's key components, features and specifications. It also tells you how to set up the board for operation.

2.1 Overview

The evaluation board consists of a baseboard (with one Intel® Pentium® III processor populated), 815E chipset, and other system board components and peripheral connectors.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals. Since the board is not in a protective chassis, take extra precaution when handling and operating the system.

2.1.1 Baseboard Features

Note: ABIT manufactured the Intel® 815E Scalable Performance Board in compliance with Rev. 0.93 of the Intel® 815E Chipset Platform Design Guidelines.

The evaluation board features are summarized below:

CPU

- Supports both Intel® Celeron™ Processors (566 MHz and above) and Intel® Pentium® III processors (up to 1 GHz); both in the flip chip-pin grid array (FC-PGA) package.
- Supports a 66, 100, or 133 MHz processor system bus (PSB).

Intel 815E Chipset

- 82815 Graphics and Memory Controller Hub (GMCH)
- 82801BA I/O Controller Hub 2 (ICH2)
- 82802AC Firmware Hub (FWH)
- Supports Ultra ATA 100/66/33 IDE protocol
- Supports AGP 2.0 including 4x AGP data transfers

Memory Support

- 100/133 MHz system memory interface
- Three 168-pin DIMM sockets support SDRAM (3.3 V, non-ECC) modules
- Supports 8-Mbyte to 512-Mbyte using 16 Mbit/64 Mbit/128 Mbit/256 Mbit technology

Flash System BIOS ROM

- General Software system BIOS

Power Supply/Management

- Standard ATX power supply connector
- SMRAM space remapping to A0000H (128 Kbyte)
- Optional Extended SMRAM space above 256 Mbyte, additional 512 Kbyte/1 Mbyte TSEG from top of memory, cacheable
- Stop clock grant and halt special cycle translation from the host to the hub interface
- APIC buffer management

Accelerated Graphics Port (AGP) Support

- AGP Interface Specification Rev 2.0 compliant
- Backward compatible with the AGP 1.0
- Single AGP 1X, 2X, 4X, 3.3 V/1.5 V device support

System I/O

- One floppy connector supporting up to 2.88 Mbytes, and three-mode floppy drives
- Two Ultra ATA 100/66/33 IDE connectors supporting up to four IDE devices
- Built-in standard/EPP/ECP parallel port connector
- Two built-in 16550 fast UART compatible serial port connectors
- Two built-in Universal Serial Bus (USB) connectors
- Built-in PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors
- One built-in VGA connector
- Built-in audio connectors (Line-in, Line-out, MIC-in) with Yamaha Audio CODEC
- One built-in game port
- Built-in audio line-in headers (CD1, CD2, and AUX1)

Peripheral Connectors

- Three PCI expansion slots
- One Communication Network Riser (CNR) slot
- One AGP slot
- ABIT V-Bus* connector accepts expansion card for video output capability (TV-Out)

Miscellaneous Features

- Micro ATX form factor
- Two built-in SMBus headers
- Built-In standard IrDA TX/RX header

- Built-in Wake On LAN (WOL) header
- Three built-in FAN power connectors (FAN1, FAN2 and FAN3)
- Power/Reset jumpers
- Jumper to select PSB speed (66, 100, or 133 MHz)
- Jumper to clear CMOS

2.2 Included Hardware

- Evaluation board (baseboard) with battery
- Intel N82802AC8 Firmware Hub
- One 866 MHz Intel® Pentium® III Processor with a 133 MHz PSB
- One 850 MHz Intel® Celeron™ Processor with a 100 MHz PSB
- One fansink thermal solution
- One 128-Mbyte PC133 SDRAM (168-pin)
- Western Digital ATA66 hard disk drive pre-loaded with an evaluation copy of BlueCat* Linux from LynuxWorks*
- 80-pin ATA/66 IDE cable for the hard disk drive
- Comm port cable
- Floppy drive cable
- 82559 fast ethernet controller card

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included in your kit are described in this section.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products.Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third-party vendors.

2.3.1 Embedded BIOS for the Intel® 815E Scalable Performance Board Development Kit

The Intel® 815E Scalable Performance Board Development Kit ships pre-installed with Embedded BIOS* pre-boot firmware from General Software. Embedded BIOS provides an industry-standard BIOS platform to run any standard operating system, including DOS*, Windows* NT, NT Embedded*, Windows 95/98, Windows CE, QNX*, VxWorks*, and Linux* among others. The Embedded BIOS Application Kit (available through General Software) includes complete source code, a reference manual, and a Windows-based expert system, BIOStart*, to enable easy and rapid configuration of customized firmware for your Intel**®** 815E Scalable Performance Board Development Kit.

The following features of Embedded BIOS have been enabled in the Intel® 815E Scalable Performance Board Development Kit:

- SDRAM detection, configuration, and initialization
- Intel® 815E chipset configuration
- Firmware Hub
- Post codes displayed to port 80H
- Two serial ports, one EPP/ECP parallel port
- PCI bus and device enumeration and configuration
- AGP configuration and initialization
- SMC LPC Super I/O programming
- Pentium® III processor microcode update
- Integrated debugger
- Burn-in diagnostics
- Console redirection
- Manufacturing mode

2.3.2 Software

2.3.2.1 BlueCat* Linux

The drive comes pre-loaded with BlueCat Linux. Some of the features of the BlueCat Linux include:

- A development environment and an operating system for embedded deployment that lets developers combine specialized, custom-developed software and hardware with off-the-shelf, third-party Linux applications.
- Configuration to accurately match the requirements of embedded development from small devices to large-scale multi-processor systems. BlueCat Linux includes a royalty-free, open source Linux distribution, enhanced with LynuxWorks' cross-development and embedding tools that improve quality and reduce development time.
- Stabilization to ensure that a consistent development and deployment environment is available for the complete lifecycle of an embedded product

- A selected subset of the standard Linux distribution tailored for embedded development and deployment, with LynuxWorks cross-development and embedding tools. Components are selected to ensure functionality, reliability, and maintainability, both on the host and target side. BlueCat Linux is configurable to meet varied requirements for kernel size, hardware configurations, boot method, and other embedded requirements. It uses the Red Hat Package Manager (RPM) to allow customized installations on the development system.

2.3.2.2 Wind River's VxWorks* Real-Time Operating System (RTOS)

wind microkernel

- Efficient task management
  - — Multitasking, unlimited number of tasks
  - — Preemptive and round-robin scheduling
  - — Fast, deterministic context switching
  - — 256 priority levels
- Fast, flexible intertask communications
  - — Binary, counting and mutual exclusion semaphores with priority inheritance
  - — Message queues
  - — POSIX pipes, counting semaphores, message queues, signals and scheduling
  - — Control sockets
  - — Shared memory
- High scalability
- Incremental linking and loading of components
- Fast, efficient interrupt and exception handling
- Optimized floating-point support
- Dynamic memory management
- System clock and timing facilities

Networking support

- BSD 4.4 TCP/IP networking
- IP, IGMP, CIDR, TCP, UDP, ARP
- RIP v.1/v.2
- Standard Berkeley sockets, zbufs (a.k.a., zero-copy sockets)
- SLIP, CSLIP, PPP
- BOOTP, DNS, DHCP, TFTP
- NFS, ONC RPC
- FTP, rlogin, rsh, telnet
- SNTP

- WindNet SNMP v.1/v.2c with MIB compiler—optional
- WindNet OSPF v.2—optional

Fast, flexible I/O and local file system

- SCSI support
- MS-DOS compatible file system
- Raw disk file system
- TrueFFS flash file system—optional
- ISO 9660 CD-ROM file system
- PCMCIA support

Target Development Features

- Full ANSI C compliance and enhanced C++ features for exception handling and template support
- Extensive POSIX 1003.1, .1b compatibility
- Interactive C interpreter target shell
- Symbolic debugging and disassembly
- Powerful performance monitoring
- Extensive kernel, task and system information utilities
- Dynamic linking loader
- Libraries of over 1800 utility routines
- Flexible booting from ROM, local disk, or over the network
- Highly scalable design allows for a wide range of applications
- System-level debugging via Ethernet, serial line, ICE, or ROM emulator

Supported VxWorks 5.x Targets

- PowerPC
- 68K, CPU 32
- ColdFire
- MCORE
- 80x86 and Pentium
- i960
- ARM and StrongARM
- MIPS
- SH
- SPARC
- NEX V8xx
- M32 R/D

- RAD6000
- ST 20
- TriCore

2.3.3 Information/Drivers CD

ABIT, the manufacturer of the baseboard, has provided a CD that contains drivers for the standard versions of the Windows operating systems (Windows 95/98/NT/2000). The CD includes drivers for on-board audio, on-board video and Intel® ATA/66. In addition, there are a few other utilities provided that may be useful. For updated drivers, refer to:

http://developer.intel.com/design/chipsets/815e/index.htm

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor: You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.

Keyboard: You need a keyboard with a PS/2-style connector or adapter.

Mouse: Optional. You can use a mouse with a PS/2-style connector or adapter.

Hard Drives andFloppy Drives: You can connect up to four IDE drives and two floppy drives to the evaluation board. Two devices (master and slave) can be attached to each IDE connector. Only one hard drive is included in your kit, so you will need to provide the cables for any additional drives. You may have all these storage devices attached to the board at the same time.

Video Adapter: You can use the integrated video adapter supplied with your kit, or you can choose to install a PCI or AGP video adapter. It is your responsibility to install the correct driver software for any video adapters other than the one provided. Check the BIOS for the proper video settings (AGP/onboard or PCI).

Network Adapter: A network interface card is included in the evaluation kit. You may use a different network card other than the card included in the kit; you are responsible for installing the correct drivers for such a network card. The evaluation board supports all standard PCI-compatible network cards. You must supply a network cable to connect to the LAN connector or any other network card you chose to install.

Power Supply: You must use a standard ATX power supply.

Other Devices and Adapters: The evaluation board functions much like a standard desktop computer motherboard. Most PC compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or an AGP graphics card.

2.5 Setting up the Evaluation Board

Once you have gathered the hardware described in section Section 2.4, follow the steps below to set up your evaluation board. This manual assumes you are familiar with the basic concepts involved with installing and configuring hardware for a personal computer system. Refer to Figure 3 on page 32 for locations of connectors, jumpers, etc.When installing drives/devices on the baseboard, refer to Figure 4 on page 33 for the correct orientation of the connecting cable.

Note: The location of pin1 on the COM2 header is **INCORRECT** in the ABIT *Brief Installation Guide ver. 1.00* (included on the ABIT drivers CD). It has been corrected in this manual.

1. Create a safe work environment.

   Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge damage, and such damage may cause product failure or unpredictable operation.

2. Inspect the contents of your kit.

   Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Note: The evaluation board is a standard micro-ATX form factor. An ATX chassis may be used if a protected environment is desired.

3. Check the jumper settings.

   JP1 is used to clear the CMOS memory (pin 2 and 3). Make sure this jumper is set for normal operation (jumper pins 1 and 2). Refer to Section 4.4.2, “CMOS (JP1)” on page 46.

4. Check the dip switch settings.

   Make sure the board’s DIP switch is configured to the correct PSB. SW1 DIP switch settings are shown in Table 20 on page 47.

5. Make sure the following hardware is populated on your evaluation board:

   — One 866 MHz Intel® Pentium® III processor

   — One 128-Mbyte PC133 SDRAM DIMM (168-pin)

   — One fan (thermal solution)

   — One network interface card

6. Install the IDE hard disk drive included in your kit:
   The evaluation board supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When using a single IDE device with the evaluation board, ensure that the jumpers are set correctly for single drive operation. For jumper settings for different configurations, consult the drive’s documentation.

   — Connect the hard drive’s IDE cable connector to the IDE1 connector on the evaluation board.

— Connect the other end of the cable to the hard disk drive.

— Connect a power cable to the hard drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation board or the hard disk.

7. Connect any additional storage devices to the evaluation board.

Note: The hard disk is already formatted and is pre-loaded with a customized target image of BlueCat Linux by LynuxWorks.

8. Connect a Floppy drive (optional).

   — Insert a floppy cable into FDC1 (be sure to orient pin 1 correctly).

   — Connect the other end of the ribbon cable to the floppy drive.

   — Connect a power cable to the floppy drive.

9. Connect the keyboard and mouse.

   Connect a PS/2-style mouse and keyboard (see Figure 3 on page 32 for connector locations).

Note: U1 (on the baseboard) is a stacked PS/2 connector. The bottom connector is for the keyboard and the top is for the mouse.

10. Connect the Ethernet adapter provided in your kit (optional).
11. Connect the audio speakers (optional).

    For audio, connect the audio speakers to the on-board line out connector.

12. Connect the power supply.

    Connect an ATX power supply to the evaluation board. Make sure the power supply is not plugged into the wall (turned off). Insert the board connector of the power supply cord into the ATXPR1 power supply header on the evaluation board. After connecting the power supply board connector to the ATXPR1 header, plug the power supply cord into the wall.

13. Power up the board.

Power and reset are implemented on the evaluation board through jumpers located on PN1 and PN2.

Power Jumper:	The power jumper consists of pins 10 and 11 on PN1. (See Figure 5 on page 46.) To power on the evaluation board, briefly short pins 10 and 11, then, release the short. (To power off, short pins 10 and 11 for about five seconds, until the power shuts off.)
Reset Jumper:	The reset jumper consists of pins 1 and 2 on PN2. (See Figure 5 on page 46.) To reset the evaluation board, short pins 1 and 2 until the board resets, and then release the short.

Turn on the power to the monitor and evaluation board. Ensure that the fansink on the processor is operating.

2.6 Configuring the BIOS

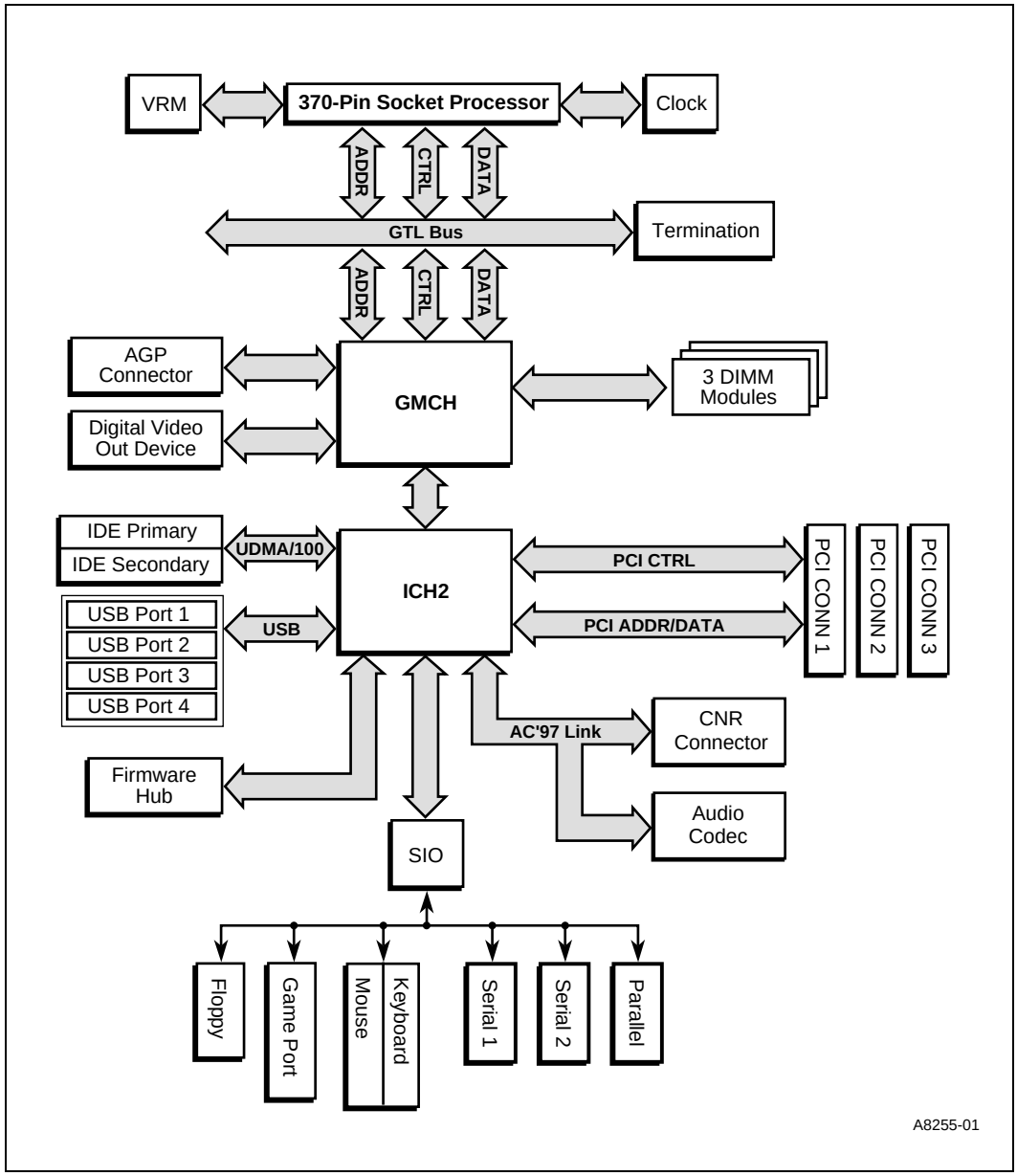
General Software's BIOS is pre-loaded on the evaluation board. You will need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Quick Reference" contains a description of BIOS options. BIOS updates may periodically be posted to Intel's Developers' Web site at:

http://developer.intel.com/design/intarch/devkits/

Theory of Operation 3

3.1 Block Diagram

Figure 1. Block Diagram



3.2 Mechanical Design

The evaluation board conforms to the micro-ATX form factor. For extra protection in a development environment, you may want to install the evaluation board in an ATX chassis. The evaluation board has three 32 bit/33 MHz PCI connectors, one AGP connector, one CNR connector, three SDRAM DIMM connectors, and one ABIT V-Bus connector. The system I/O connectors are in the rear of the board in the defined micro-ATX I/O window.

3.3 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements.

Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor using metal clips. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.4 System Operation

The Intel® 815E Scalable Performance Board Development Kit is designed to support Intel® Celeron™ processors (566 MHz and above) and Intel® Pentium® III processors up to 1 GHz in the flip chip-grid array (FC-PGA) package. The 815E chipset includes the GMCH, ICH2, and the FWH.

3.4.1 Intel® Pentium® III Processor

The Intel® Pentium® III processor is a member of the P6 family in the Intel® IA-32 processor line. Like the Intel® Pentium® II processor, the Intel® Pentium® III processor implements the Dynamic Execution microarchitecture — a unique combination of multiple branch prediction, data flow analysis, and speculative execution. Intel® Pentium® III processor features include the following:

- Dynamic Execution technology
- Includes Intel MMX media enhancement technology
- Intel streaming SIMD extensions
- Incorporates separate 16 Kbyte level-one caches (32 Kbytes total); one for instructions and one for data
- 256 Kbytes integrated, full-speed level two cache with error correcting code (ECC)
- 8-way level two cache associativity, which provides improved cache-hit rate on read/store operations
- Double quad word-wide (256 bit) cache data bus, which provides extremely high throughput on read/store operations

- Support for 66 MHz, 100 MHz and 133 MHz processor system bus frequencies
- Intel® processor serial number

3.4.2 Intel® Celeron™ Processor

The Intel® Celeron™ processor family delivers quality, reliability, and compatibility while offering good performance for today's most widely-used applications. Intel® Celeron™ processor features include:

- Dynamic Execution technology
- Includes Intel MMX* media enhancement technology
- Intel streaming SIMD extensions
- Incorporates separate 16 Kbyte level-one caches (32 Kbytes total); one for instructions and one for data
- Incorporates a 128 Kbyte unified, non-blocking, level-two cache that improves performance by reducing the average memory access time and providing fast access to recently used instructions and data
- 66/100 MHz Intel® P6 micro-architecture's multi-transaction system bus that supports multiple outstanding transactions to increase bandwidth availability
- A pipelined Floating-Point Unit (FPU) for supporting the 32-bit and 64-bit formats specified in IEEE standard 754, as well as an 80-bit format
- Parity-protected address/request and response system bus signals with a retry mechanism for high data integrity and reliability

3.4.3 Intel® 815E Chipset

3.4.3.1 Graphics and Memory Controller Hub (GMCH)

The GMCH provides the processor interface (optimized for Intel® Pentium® III processors and Intel® Celeron™ processors), DRAM interface, hub interface and an AGP interface or internal graphics. It provides flexibility and scalability in graphics and memory subsystem performance.

GMCH features:

- 544 BGA package
- 66, 100, or 133 MHz Processor System Bus
- 32-bit host bus addressing
- Four deep in-order queue
- Processor support
  - — Celeron™ processor (128 Kbytes) in 370-pin FC-PGA package
  - — Pentium® III processor (256 Kbytes) in 370-pin FC-PGA package

- System DRAM controller
  - — Three DIMM slots
  - — 100/133 MHz clock
- Accelerated hub architecture
- Digital video out port
- AGP 1X/2X/4X port

3.4.3.2 I/O Controller Hub (ICH2)

The Intel 82801BA I/O Controller Hub (ICH2) is a highly integrated multifunctional I/O controller hub that provides the interface to the PCI bus and integrates many of the functions needed in today's PC platforms. The ICH2 communicates with the host controller over a dedicated hub interface.

ICH2 Features:

- PCI 2.2 with six PCI REQ/GNT pairs
- Eight PCI interrupts
- AC'97 2.1 with six channel audio support
- LPC interface
- Wake-On-LAN support
- System management
- 21 GPIO signals
- Interrupt controller
- 82C54-based timer
- ACPI compliant
- RTC
- 360 eBGA package
- Four IDE @ ATA 100 max
- Two USB 1.1 controllers providing four ports
- Enhanced SMBus with slave interface
- Integrated MAC

3.4.3.3 Firmware Hub (FWH)

The Firmware Hub (FWH) stores system BIOS and video BIOS, as well as an Intel® Random Number Generator (RNG). The Intel RNG provides truly random numbers to enable stronger encryption, digital signing and security protocols. The FWH is key to enabling future security and manageability infrastructures.

FWH Features:

- 32-pin PLCC package
- 8-Mbit flash memory

- Symmetrically-blocked flash memory array (64 Kbyte)
- Pin and register-based block locking
- Integrated hardware RNG
- Single-byte read/write
- Five GPIs

3.4.4 System Memory SDRAM

Memory Features:

- Three 168-pin SDRAM DIMM sockets
- Supports 8 Mbyte to 512 Mbyte using 16 Mbit/64 Mbit/128 Mbit/256 Mbit technology
- Supports 100/133 MHz system memory bus

3.4.5 Boot ROM

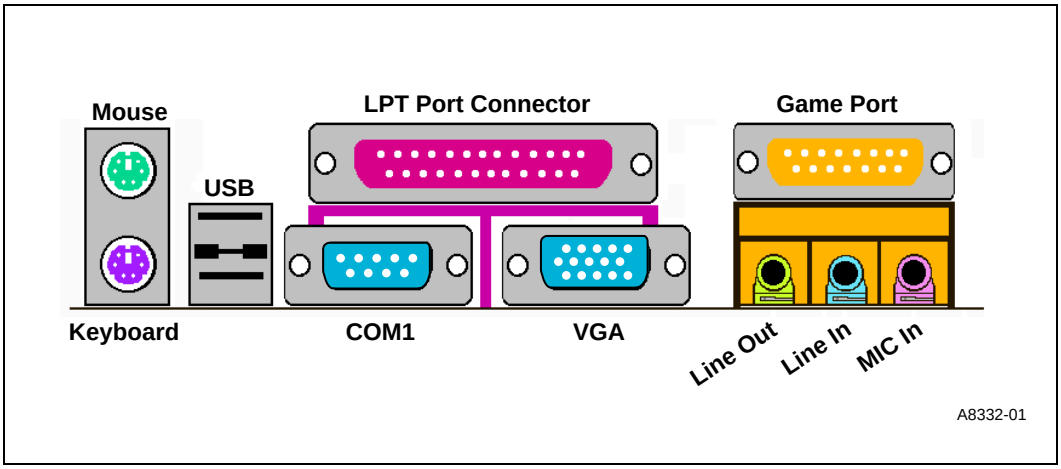
The system boot ROM installed at U23 is the Intel® FWH, N82802AC8 device. The FWH is socketed and is addressable on the LPC bus off of the ICH2.

3.4.6 System I/O

The evaluation board contains the following I/O devices.

- Single floppy controller support
- Primary and secondary IDE interface (supports four drives)
- Two serial ports
- One parallel port
- Two USB ports
- VGA connector
- AC’97 specification compliant audio
- Line Out, Line IN, and MIC IN connectors
- MIDI/game port
- PS/2-style keyboard and mouse ports

Figure 2. Back Panel I/O Connectors



3.4.6.1 Floppy Disk Drive Support

One 34-pin floppy connector is provided on the evaluation board.

3.4.6.2 IDE Support

The evaluation board supports both a primary and secondary IDE interface via two 40-pin IDE connectors. IDE1 is the primary interface and IDE2 is the secondary interface.

3.4.6.3 RS-232 Serial Ports

The evaluation board provides one built-in serial port (COM1) and a header for an additional serial port (COM2). COM1 is attached to the back panel I/O connector. COM2 is a header that connects to a serial port cable to provide the additional serial port.

3.4.6.4 IEEE 1284 Parallel Port

One 25-pin DSUB IEEE 1284 parallel port is provided (LPT1).

3.4.6.5 USB Ports

The evaluation board provides two USB connectors (USB1).

3.4.6.6 VGA Connector

This connector is a 15-pin DSUB female connector for output to a monitor.

3.4.6.7 Audio Subsystem

The evaluation board has an integrated (on-board) AC'97 compliant subsystem.

Audio Subsystem Features:

- Line input (back panel)
- Line output (back panel)
- Microphone input (back panel)

3.4.6.8 Game Port Connector

The game port connector is a standard 15-pin DSUB connector for attaching a joystick, game pad or other MIDI device.

3.4.6.9 Keyboard/Mouse

The keyboard and mouse connectors (U1) are PS/2 style, 6-pin stacked miniature DSUB connectors. The top connector is for the mouse and the bottom connector is for the keyboard.

3.4.7 Expansion Connectors

The evaluation board contains the following expansion connectors:

- One AGP 4x slot
- Three PCI 32/33 slots
- One CNR slot
- One V-Bus connector

3.4.7.1 AGP Connector

AGP support is provided through the 82815 GMCH. One industry standard AGP connector (AGP1) is provided on the evaluation board. The AGP connector can accept a Graphics Performance Adapter (GPA) to enhance system graphics performance by providing dedicated display cache for internal graphics.

AGP Features:

- AGP 1X, 2X, and 4X transfer rates
- Differential strobes for more accurate timing

Dual mode buffers allow the use of 1.5 V and 3.3 V compliant devices.

AGP add-in cards must comply with the Rev. 2.0 *Accelerated Graphics Port Specification*.

3.4.7.2 32-bit/33-MHz PCI Connectors

Three industry standard 32-bit/33-MHz PCI connectors (PCI1, PCI2, and PCI3) are provided on the evaluation board.

3.4.7.3 CNR Connectors

One CNR connector is included on the board. Intel® has not validated this feature.

3.4.7.4 V-Bus Connector

A V-BUS TV-out adapter can be installed in this connector (VL1), which has general video output and S-Video out for display on a TV monitor. Intel has not validated this feature. Contact ABIT* for more information.

3.4.8 Post Code Debugger

An on-board Post-Code Debugger is not implemented on the evaluation board. However, post code debugging can be accomplished through the use of a port 080H expansion card.

3.4.9 Clock Generation

The clock synthesizer on the baseboard generates and distributes the clocks used by the entire system.

3.4.9.1 System Clocks

The CK Intel® 815E Chipset: 3 DIMM Clock Synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Intel® 815E Scalable Performance Board Development Kit:

CPU	66 MHz/100 MHz/133 MHz
PCI	33 MHz
SDRAM	100 MHz/133 MHz
3V66	66 MHz (3.3 V)
USB	48 MHz
DOT	48 MHz
REF	14.31818 MHz
APIC	33 MHz

3.4.10 Power Supply Requirements

The Intel® 815E Scalable Performance Board uses a standard ATX power supply.

3.5 Battery Requirements

A type 2032, socketed, 3 V lithium coin cell battery is used on this evaluation board. The battery has a shelf life of greater than three years.

Hardware Reference 4

This section provides reference information on the hardware, including connector pinout information and jumper settings.

4.1 Thermal Management

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor using metal clips. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

For additional thermal design information refer to the following documents:

- *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1.0B GHz Datasheet* (order number 245264)
- *Intel® Pentium® III Processor Thermal Design Guide* (order number 273325)
- *Intel® Celeron™ Processor up to 850 MHz* datasheet (order number 243658)
- *Intel® Celeron™ Processor Thermal Design Guide (*order number 273421)

4.2 Post Code Debugging

The evaluation board does not have an on-board post code display. However, post code debugging can be accomplished through the use of a Port 080H expansion card. These cards are available from various vendors. One such vendor is PC Engines (www.pcengines.com).

4.3 Connector Pinouts

Figure 3. Baseboard Layout Diagram

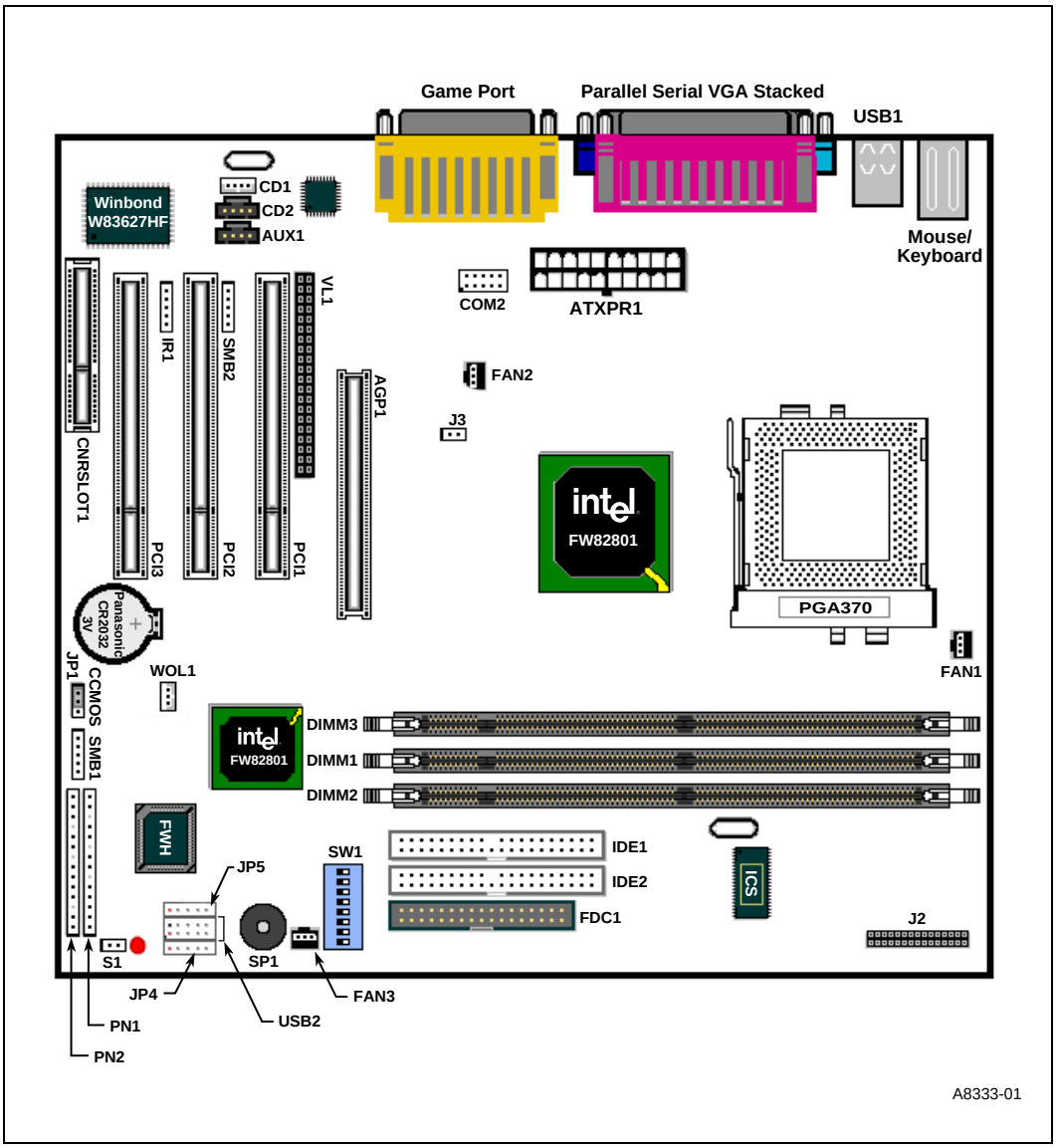
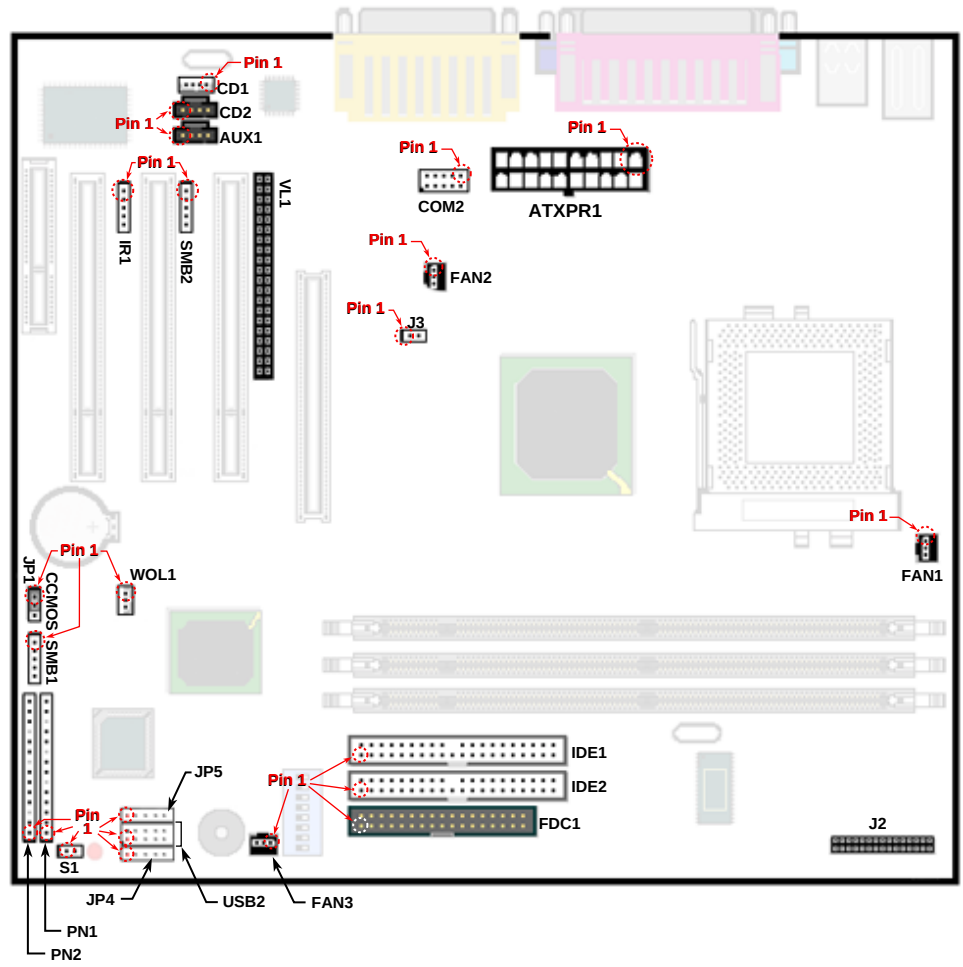


Figure 4. Baseboard Connector Orientation



4.3.1 ATX Power Connector

Table 2 shows the signals assigned to the ATX style power connector.

Table 2. Power Connector (ATXPR1)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5V	+5 V VCC
5	GND	Ground
6	+5 V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	-12 V	-12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	-5 V	-5 V
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.3.2 Dual Stacked USB Connector

Table 3 shows the signals assigned to the dual stacked USB connector (USB1).

Table 3. USB Connector Pinout (USB1)

Pin	Signal Name
1,5	Power (fused)
2,6	USBP0# [USBP1#]
3,7	USBP0 [USBP1]
4,8	GND

4.3.3 PS/2-Style Mouse and Keyboard Connectors

Table 4 shows the signals assigned to the keyboard and mouse connector (U1). The mouse port is on the top and the keyboard port is on the bottom.

Table 4. PS/2-Style Mouse and Keyboard Pinout (U1)

Pin	Signal Name
1	Data
2	No Connect
3	GND
4	+5 V (fused)
5	Clock
6	No Connect

4.3.4 VGA Port

Table 5. VGA Connector Pinout (VGA)

Pin	Signal
1	RED
2	GREEN
3	BLUE
4	N/C
5	GND
6	ANALOG GND
7	ANALOG GND
8	ANALOG GND
9	N/C
10	GND
11	N/C
12	N/C
13	H SYNC
14	V SYNC
15	N/C

4.3.5 Parallel Port

Table 6 shows the signals assigned to the parallel port connector (LPT1).

Table 6. Parallel Port Connector Pinout (LPT1)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLC IN#
5	Data Bit 3	18	GND
6	Data Bit 4	19	GND
7	Data Bit 5	20	GND
8	Data Bit 6	21	GND
9	Data Bit 7	22	GND
10	ACK#	23	GND
11	Busy	24	GND
12	Paper end	25	GND
13	SLCT		

4.3.6 Serial Ports

Table 7 shows the signals assigned to the serial port connectors (COM1 and COM2). COM1 is attached to the back panel I/O connector. COM2 is a serial COM port. If you have a serial port bracket, it can be connected to COM2 for one additional serial port.

Table 7. Serial Port Connector Pinout (COM1 and COM2)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.3.7 Audio Connectors

Refer to Figure 2 on page 26 for the connectors referenced in this section.

Table 8 shows the signals assigned to the audio line-out connector.

Table 8. Audio Line-Out Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Audio Left Out
Ring	Audio Right Out

Table 9 shows the signals assigned to the audio line-in connector.

Table 9. Audio Line-In Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Audio Left In
Ring	Audio Right In

Table 10 shows the signal assigned to the audio mic-in connector.

Table 10. Audio Mic-In Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Mono In
Ring	Mic bias voltage

Table 11 shows the signals assigned to the MIDI/game port connector.

Table 11. MIDI/Game Port Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4	10	GP6
3	GP0	11	GP2
4	GND	12	MIDI-OUTR
5	GND	13	GP3
6	GP1	14	GP7
7	GP5	15	MIDI-INR
8	+5 V (fused)	16	NC

4.3.8 Wake On LAN (WOL)

Table 12 shows the signals assigned to the Wake-ON-LAN (WOL) connector (WOL1).

Table 12. Wake-ON-LAN Connector Pinouts (WOL1, not populated)

Pin	Signal Name
1	5 VSB
2	Ground
3	WOL

4.3.9 Front Panel I/O Connectors

Table 13 shows the signals assigned to the front panel I/O connectors (PN1 and PN2).

Table 13. Front Panel I/O Connectors

PN1		PN2	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	Power LED	1	Reset
2	Power LED	2	Reset
3	Power LED	3	No Pin
4	Keylock	4	Speaker
5	Keylock	5	Speaker
6	No Pin	6	Speaker
7	HDD LED	7	Speaker
8	HDD LED	8	No Pin
9	No Pin	9	SP LED
10	Power ON	10	SP LED
11	Power ON	11	No Pin
12	No Pin	12	Reserve
13	SMI	13	Reserve
14	SMI	14	Reserve

4.3.10 IDE Connector

Table 14 shows the signals assigned to the IDE connectors (IDE1 and IDE2).

Table 14. IDE Connector Pinouts for IDE1 and IDE2 (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	21	DRQ3
2	Ground	22	Ground
3	Host Data 7	23	I/O Write#

Table 14. IDE Connector Pinouts for IDE1 and IDE2 (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name
4	Host Data 8	24	Ground
5	Host Data 6	25	I/O Read#
6	Host Data 9	26	Ground
7	Host Data 5	27	IOCHRDY
8	Host Data 10	28	BALE
9	Host Data 4	29	DACK3#
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ14
12	Host Data 12	32	IOCS16#
13	Host Data 2	33	Addr1
14	Host Data 13	34	Ground
15	Host Data 1	35	Addr 0
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Select 0#
18	Host Data 15	38	Chip Select 1#
19	Ground	39	Activity
20	Key	40	Ground

4.3.11 Floppy Drive Connector

Table 15 shows the signals assigned to the floppy drive connector (FDC1).

Table 15. Floppy Drive Connector Pinouts (FDC1) (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	FDHDIN
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#

Table 15. Floppy Drive Connector Pinouts (FDC1) (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.3.12 32-Bit PCI Slot Connector

Table 16 shows the signals assigned to the 32-Bit PCI slot connectors (PCI1, PCI2, and PCI3).

Table 16. 32-Bit PCI Slot Connector Pinouts (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VCC	B1	-12 V	A32	AD16	B32	AD17
A2	+ 12 V	B2	GND	A33	3.3 V	B33	CBE2#
A3	VCC	B3	GND	A34	FRAME#	B34	GND
A4	VCC	B4	No Connect	A35	GND	B35	IRDY#
A5	VCC	B5	VCC	A36	TRDY#	B36	3.3 V
A6	PIRQ1#	B6	VCC	A37	GND	B37	DEVSEL#
A7	PIRQ3#	B7	PIRQ2#	A38	STOP#	B38	GND
A8	VCC	B8	PIRQ0	A39	3.3 V	B39	LOCK#
A9	No Connect	B9	PRSNT1B #	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3V
A11	No Connect	B11	PRSNT2B #	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3 V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	Reserved	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3 V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5

Table 16. 32-Bit PCI Slot Connector Pinouts (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3#	A57	AD2	B57	GND
A27	3.3 V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	VCC	B59	VCC
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	VCC	B61	VCC
A31	AD18	B31	3.3 V	A62	VCC	B62	VCC

4.3.13 4.5.11 AGP Connector

Table 17 shows the signals assigned to the AGP connector (AGP1).

Table 17. AGP Connector Pinouts (Sheet 1 of 2)

Pin	Signal		Pin	Signal	
1	12 V	OVRCNT#	34	3.3 Vddq	3.3 Vddq
2	TYPEDET#	5.0V	35	AD22	AD21
3	Reserved	5.0V	36	AD20	AD19
4	USB-	USB+	37	GND	GND
5	GND	GND	38	AD18	AD17
6	INTA#	INTB#	39	AD16	C/BE2#
7	RST#	CLK	40	3.3 Vddq	3.3 Vddq
8	GNT#	REQ#	41	FRAME#	IRDY#
9	3.3 VCC	3.3 VCC	42	Reserved	3.3 Vaux
10	ST1	ST0	43	GND	GND
11	Reserved	ST2	44	Reserved	Reserved
12	PIPE#	RBF#	45	3.3 VCC	3.3 VCC
13	GND	GND	46	TRDY#	DEVSEL#
14	Reserved	Reserved	47	STOP#	3.3 Vddq
15	SBA1	SBA0	48	PME#	PERR#
16	3.3 VCC	3.3 VCC	49	GND	GND
17	SBA3	SBA2	50	PAR	SERR#
18	Reserved	SB_STB	51	AD15	C/BE1#
19	GND	GND	52	3.3 Vddq	3.3 Vddq
20	SBA5	SBA4	53	AD13	AD14
21	SBA7	SBA6	54	AD11	AD12
22	KEY	KEY	55	GND	GND

Table 17. AGP Connector Pinouts (Sheet 2 of 2)

Pin	Signal		Pin	Signal	
23	KEY	KEY	56	AD9	AD10
24	KEY	KEY	57	C/BE0#	AD8
25	KEY	KEY	58	3.3 Vddq	3.3 Vddq
26	AD30	AD31	59	Reserved	AD_STB0
27	AD28	AD29	60	AD6	AD7
28	3.3 VCC	3.3 VCC	61	GND	GND
29	AD26	AD27	62	AD4	AD5
30	AD24	AD25	63	AD2	AD3
31	GND	GND	64	3.3 Vddq	3.3 Vddq
32	Reserved	AD_STB1	65	AD0	AD1
33	C/BE3#	AD23	66	Reserved	Reserved

NOTES:

1. Reserved pins are only for future use by the AGP interface specification.
2. IDSEL# is not a pin on the AGP connector. AGP graphics components should connect the AD16 signal to the 3.3 V IDSEL# function internal to the component.
3. All 3.3 V cards leave the TYPEDET signal open. All 1.5 V cards tie this signal hard to ground.

4.3.14 CNR Connector

Table 18 and Table 19 shows the signals assigned to the Type A and Type B CNR connectors (CNRSLOT1).

Table 18. Pin Assignment for the Type A CNR Connector, using the 8-pin LAN Interface

Pin	Signal Name	Signal Name	Pin
B1	RESERVED	RESERVED	A1
B2	RESERVED	RESERVED	A2
B3	RESERVED	GND	A3
B4	GND	RESERVED	A4
B5	RESERVED	RESERVED	A5
B6	RESERVED	GND	A6
B7	GND	LAN_TXD2	A7
B8	LAN_TXD1	LAN_TXD0	A8
B9	LAN_RSTSYNC	GND	A9
B10	GND	LAN_CLK	A10
B11	LAN_RXD2	LAN_RXD1	A11
B12	LAN_RXD0	RESERVED	A12
B13	GND	USB+	A13
B14	RESERVED	GND	A14
B15	+5 Vdual	USB-	A15
B16	USB_OC#	+12 V	A16
B17	GND	GND	A17
B18	-12 V	+3.3 Vdual	A18
B19	+3.3VD	+5VD	A19
KEY			
B20	GND	GND	A20
B21	EE_DOUT	EE_DIN	A21
B22	EE_SHCLK	EE_CS	A22
B23	GND	SMB_A1	A23
B24	SMB_A0	SMB_A2	A24
B25	SMB_SCL	SMB_SDA	A25
B26	CDC_DN_ENAB#	AC97_RESET#	A26
B27	GND	RESERVED	A27
B28	AC97_SYNC	AC97_SDATA_IN1	A28
B29	AC97_SDATA_OUT	AC97_SDATA_IN0	A29
B30	AC97_BITCLK	GND	A30

Table 19. Pin Assignment for the Type B CNR Connector, using the 17-pin LAN Interface

Pin	Signal Name	Signal Name	Pin
B1	MII_MDIO	MII_MDC	A1
B2	MII_COL	MII_CRS	A2
B3	MII_TXC	GND	A3
B4	GND	MII_RXDV	A4
B5	MII_RXERR	MII_RXC	A5
B6	MII_TXD3	GND	A6
B7	GND	MII_TXD2	A7
B8	MII_TXD1	MII_TXD0	A8
B9	MII_TXEN	GND	A9
B10	GND	RESERVED	A10
B11	MII_RXD2	MII_RXD1	A11
B12	MII_RXD0	MII_RXD3	A12
B13	GND	USB+	A13
B14	RESERVED	GND	A14
B15	+5Vdual	USB-	A15
B16	USB_OC#	+12 V	A16
B17	GND	GND	A17
B18	-12V	+3.3Vdual	A18
B19	+3.3 V	+5VD	A19
KEY			
B20	GND	GND	A20
B21	EE_DOUT	EE_DIN	A21
B22	EE_SHCLK	EE_CS	A22
B23	GND	SMB_A1	A23
B24	SMB_A0	SMB_A2	A24
B25	SMB_SCL	SMB_SDA	A25
B26	CDC_DN_ENAB#	AC97_RESET#	A26
B27	GND	RESERVED	A27
B28	AC97_SYNC	AC97_SDATA_IN1	A28
B29	AC97_SDATA_OUT	AC97_SDATA_IN0	A29
B30	AC97_BITCLK	GND	A30

4.4 Jumpers

4.4.1 PN1 and PN2 Headers

These headers provide the signals to the LED, power/reset button and speaker that are usually connected to the chassis when the system is mounted in a chassis.

4.4.1.1 Power LED (PN1: Pins 1—3)

An LED designed for the front panel of a chassis can be connected to these pins to show the power-on status.

4.4.1.2 Keylock (PN1: Pins 4 and 5)

On these pins you can connect a physical lock designed for a chassis, which allows you to lock your chassis with a key, so that the system cannot be turned on.

4.4.1.3 HDD-LED (PN1: Pins 7 and 8)

An LED can be attached to these pins. It shows hard disk drive activity.

4.4.1.4 Power (PN1: Pins 10 and 11)

Power is implemented on the evaluation board by pins 10 and 11 located on PN1. To power-on the evaluation board, short pins 10 and 11 until the board powers on and then release the short. To turn off the board, hold the jumper on pins 10 and 11 for four seconds.

4.4.1.5 SMI (PN1: Pins 13 and 14)

This is the hardware suspend header. Because power management is not supported on this system, these pins should remain open (unconnected).

4.4.1.6 Reset (PN2: Pins 1 and 2)

Reset is implemented on the evaluation board by pins 1 and 2 located on PN2. To reset the evaluation board, short pins 1 and 2 until the board resets and then release the short.

4.4.1.7 Speaker (PN2: Pins 4—7)

This is the header for connecting an internal PC speaker.

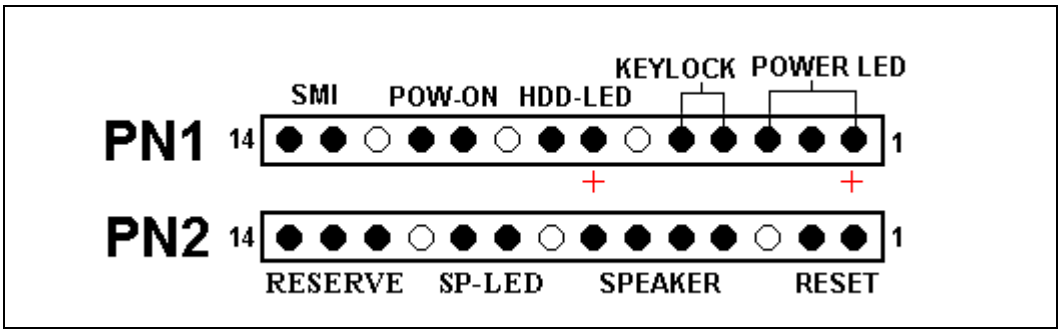
4.4.1.8 SP_LED (PN2: Pins 9 and 10)

An LED may be connected here to show the suspend state status. Because power management is not supported on this system, these pins should remain open (unconnected).

4.4.1.9 Reserve (PN2: Pins 12—14)

These pins are reserved. Do not use.

Figure 5. PN1, PN2 Diagram



4.4.2 CMOS (JP1)

JP1 controls the power to the battery backed-up CMOS memory. This CMOS memory stores system information required by the BIOS during startup. For normal operation, jumper pins 1 and 2. To clear the CMOS RAM, perform the following steps:

1. Shut down the system.
2. Disconnect the power supply (ATXPR1).
3. Remove jumper from pins 1 and 2. Short pins 2 and 3 (clear CMOS).
4. Wait 10 seconds.
5. Replace the jumper on pins 1 and 2 (normal operation).
6. Reconnect the power supply (ATXPR1).
7. Boot the system and enter the BIOS setup screen to reconfigure the system.

Short Pins 1 and 2	Normal Operation (default)
Short Pins 2 and 3	Clear saved CMOS data

4.4.3 JP3 Header

A header that allows you to connect an additional thermistor to detect the temperature at a location on the board you select.

4.4.4 CNR USB Settings (JP4 and USB2)

When using CNR's USB, these are the settings for JP4 and USB2.

- Place the jumpers across JP4 pin 3 with USB2 pin 5
- Place the jumpers across JP4 pin 4 shorted with USB2 pin 7

JP5	1	2	3	4	5
USB2	2	4	6	8	10
	1	3	5	7	9
JP4	1	2	3	4	5

4.4.5 AGP USB Settings (JP5 and USB2)

When using AGP's USB, these are the settings for JP5 and USB2.

- Place the jumpers across JP5 pin 3 with USB2 pin 6
- Place the jumpers across JP5 pin 4 with USB2 pin 8

JP5	1	2	3	4	5
USB2	2	4	6	8	10
	1	3	5	7	9
JP4	1	2	3	4	5

4.5 Processor DIP Switch Settings (SW1)

Processor settings, including PSB frequency selection, are implemented on the board by a DIP Switch (SW1).

Table 20. Processor DIP Switch Settings (Sheet 1 of 2)

Switch	On/Off	Description	Default
1-2	1:ON 2:ON	Use CPU Default Frequency Setting	Default
	1:OFF 2:ON	Reserved	
	1:OFF 2:OFF	Use SW1: 3-4 Frequency Setting	
	1:ON 2:OFF	Reserved	
3-4	3:ON 4:ON	66 MHz	
	3:OFF 4:ON	100MHz	
	3:OFF 4:OFF	133 MHz	Default
	3:ON 4:OFF	No Define	
5	ON	Use CPU Frequency Strap in ICH2 Register	
	OFF	Force CPU Frequency Strap to Safe Mod (1111)	Default
6	ON	No Reboot on 2nd Watchdog Timeout	
	OFF	Reboot on 2nd Watchdog Timeout	Default

NOTE: If you want to use SW1: 3-4 to set CPU frequency, SW1: 1-2 must be set at off.

Table 20. Processor DIP Switch Settings (Sheet 2 of 2)

Switch	On/Off	Description	Default
7	ON	Use Onboard Codec	
	OFF	Disable Onboard Codec	Default
8	--	Reserved	Default Off

NOTE: If you want to use SW1: 3-4 to set CPU frequency, SW1: 1-2 must be set at off.

BIOS Quick Reference 5

The evaluation board is licensed with a single copy of Embedded BIOS and Embedded DOS software from General Software, Inc.[1] This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the Web at http://www.gensw.com, or via e-mail at sales@gensw.com.

BIOS updates may periodically be posted to the Intel Developers' Web site at http://developer.intel.com/.

5.1 Overview

The system's pre-boot environment is managed with an adaptation of Embedded BIOS from General Software. The pre-boot environment includes POST, Setup Screen System, Manufacturing Mode, Console Redirection, Windows CE Loader (CE Ready), and Integrated BIOS Debugger. A REFLASH tool is also available to update the BIOS image with new builds of Embedded BIOS that may be obtained from General Software.

Before using the system, please read the following to properly configure CMOS settings, and learn how to use the embedded features of the pre-boot firmware, Embedded BIOS.

The last two sections of this chapter provide the BIOS POST Codes and Beep codes.

5.2 Power-On Self-Test (POST)

When the system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, POST progress codes are written by the system BIOS to I/O port 80H, allowing the user to monitor the progress with a special monitor. "Embedded BIOS POST Codes" on page 61 lists the POST codes and their meanings.

During early POST, no video is available to display error messages if a critical error is encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult "Embedded BIOS Beep Codes" on page 64 for a list of beep codes used by the system's BIOS.

5.3 The BIOS User Interface

The system BIOS can use the standard keyboard and video device, or use console redirection to demonstrate headless operation. For headless operation, remove the standard keyboard and screen devices and the system will boot unattended. If an RS232 cable is attached to COM1, a PC/AT-style character-based POST is available from HyperTerminal, PROCOMM, or any other terminal emulator software that supports VT100 emulation.

1. General Software™, the GS Logo, Embedded BIOS™, BIOStart™, CE-Ready™, and Embedded DOS™ are trademarks or registered trademarks of General Software, Inc.

When a keyboard and video device are attached, the system can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST screens accept a <DEL> key-press to enter the setup screen, and both display boot-time progress activity. The graphical display shows the status of file system devices and even OEM-defined devices (when the OEM adapts the BIOS to a particular OEM platform), but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

Figure 6 shows the format of the text-based POST display. The display is very similar if console redirection through a COM port is used instead.

Figure 6. BIOS POST Pre-Boot Environment

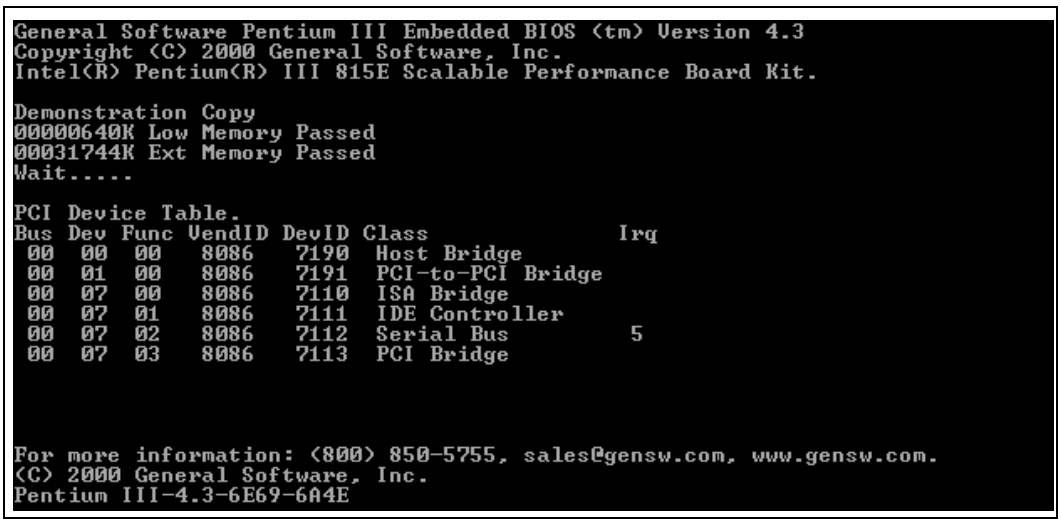
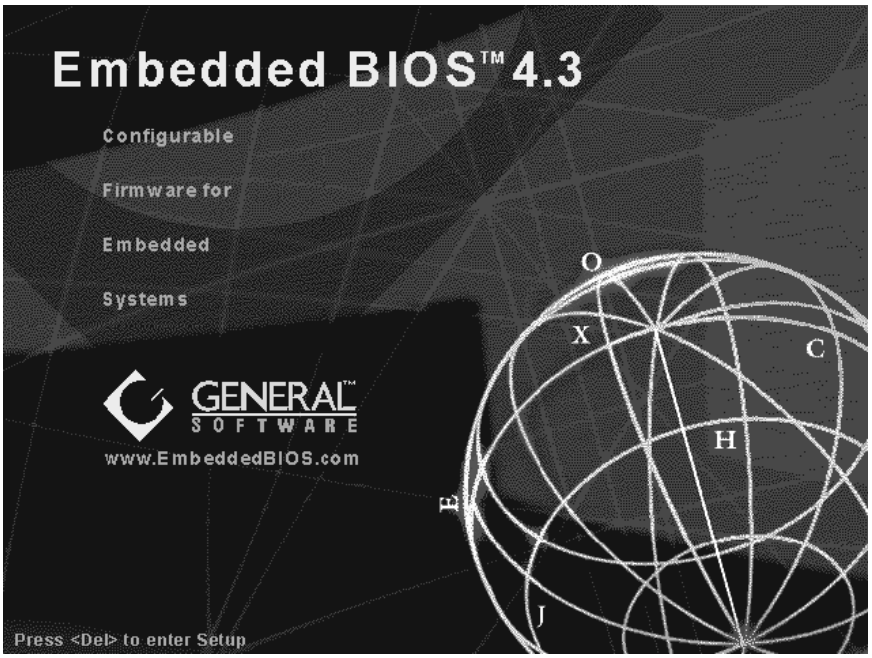

General Software Pentium III Embedded BIOS (tm) Version 4.3
Copyright (C) 2000 General Software, Inc.
Intel(R) Pentium(R) III 815E Scalable Performance Board Kit.
Demonstration Copy
00000640K Low Memory Passed
00031744K Ext Memory Passed
Wait.....
PCI Device Table.
Bus Dev Func VendID DevID Class Irq
00 00 00 8086 7190 Host Bridge
00 01 00 8086 7191 PCI-to-PCI Bridge
00 07 00 8086 7110 ISA Bridge
00 07 01 8086 7111 IDE Controller
00 07 02 8086 7112 Serial Bus 5
00 07 03 8086 7113 PCI Bridge
For more information: (800) 850-5755, sales@gensw.com, www.gensw.com.
(C) 2000 General Software, Inc.
Pentium III-4.3-6E69-6A4E

Figure 7 shows the graphical version of POST. The BIOS decompresses the main image and can display multiple overlaid graphics at various points in POST. The OEM can define the entire sequence and control the timing of the system for an embedded application, and can arrange to have different graphics displayed on each successive boot of the system. This feature is ideal for embedded systems that must show evidence of operation during startup, while the application loads underneath the splash screen. Once the application begins writing to the screen, the splash screen relinquishes control, providing a seamless graphical progression for the end user.

Figure 7. Graphical POST



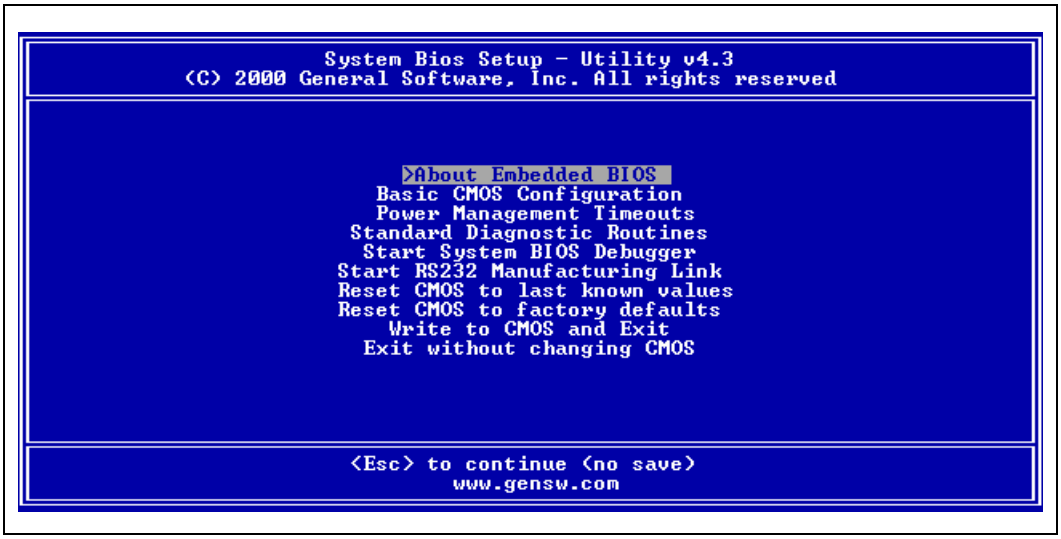
When the system is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's real time clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

The Basic Setup Screen provides an option to disable the graphical POST and switch to the legacy text-based version. This feature may not permanently disable the graphical POST if the BIOS adaptation calls for reverting to the graphical form after so many boots. If you find that the graphical POST comes back after several boots, it is because this option is enabled for this platform. The OEM can use the Embedded BIOS Adaptation Kit to control whether setup can be used to dictate the policy, and whether it is permanent or temporary.

5.4 Setup Screen System

The system is configured from within the Setup Screen System, which is a series of menus that can be invoked from POST by pressing the <DEL> key if the main keyboard is being used, or by pressing Ctrl+C if the console is being redirected to a terminal program.

Figure 8. Embedded BIOS Setup Screen Menu

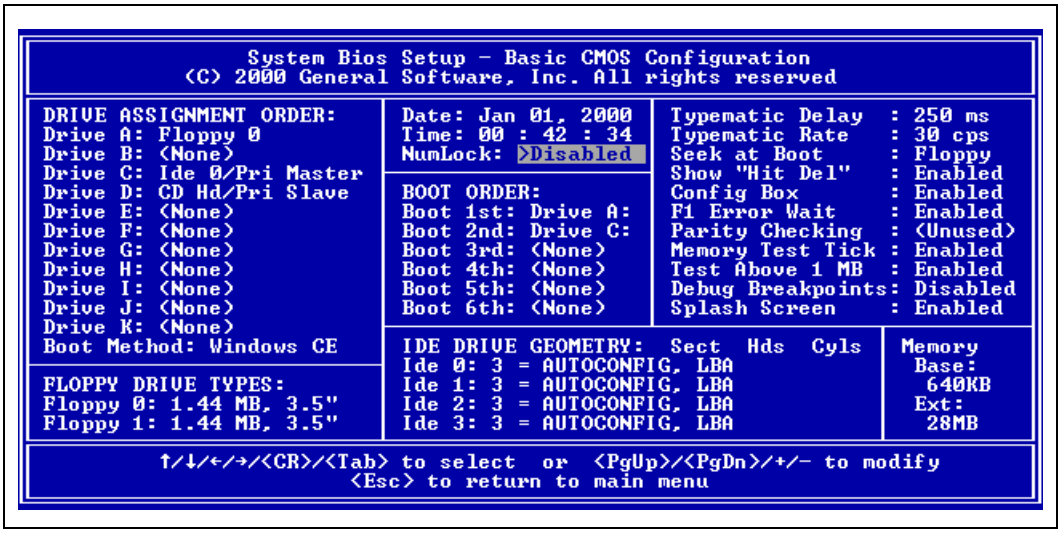

System Bios Setup - Utility v4.3
(C) 2000 General Software, Inc. All rights reserved
>About Embedded BIOS
Basic CMOS Configuration
Power Management Timeouts
Standard Diagnostic Routines
Start System BIOS Debugger
Start RS232 Manufacturing Link
Reset CMOS to last known values
Reset CMOS to factory defaults
Write to CMOS and Exit
Exit without changing CMOS
<Esc> to continue <no save>
www.gensw.com

Once in the Setup Screen System (Figure 8), the user can navigate with the UP and DOWN arrow keys from the main console, or use the Ctrl+E and Ctrl+X keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen, or the Diagnostics Setup Screen.

5.4.1 Basic CMOS Configuration Screen

The system's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 9). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 9. Embedded BIOS Basic Setup Screen


System Bios Setup - Basic CMOS Configuration
(C) 2000 General Software, Inc. All rights reserved
DRIVE ASSIGNMENT ORDER:
Drive A: Floppy 0
Drive B: (None)
Drive C: Ide 0/Pri Master
Drive D: CD Hd/Pri Slave
Drive E: (None)
Drive F: (None)
Drive G: (None)
Drive H: (None)
Drive I: (None)
Drive J: (None)
Drive K: (None)
Boot Method: Windows CE
FLOPPY DRIVE TYPES:
Floppy 0: 1.44 MB, 3.5"
Floppy 1: 1.44 MB, 3.5"
Date: Jan 01, 2000
Time: 00 : 42 : 34
NumLock: >Disabled
BOOT ORDER:
Boot 1st: Drive A:
Boot 2nd: Drive C:
Boot 3rd: (None)
Boot 4th: (None)
Boot 5th: (None)
Boot 6th: (None)
Typematic Delay : 250 ms
Typematic Rate : 30 cps
Seek at Boot : Floppy
Show "Hit Del" : Enabled
Config Box : Enabled
F1 Error Wait : Enabled
Parity Checking : (Unused)
Memory Test Tick : Enabled
Test Above 1 MB : Enabled
Debug Breakpoints: Disabled
Splash Screen : Enabled
IDE DRIVE GEOMETRY: Sect Hds Cyls
Ide 0: 3 = AUTOCONFIG, LBA
Ide 1: 3 = AUTOCONFIG, LBA
Ide 2: 3 = AUTOCONFIG, LBA
Ide 3: 3 = AUTOCONFIG, LBA
Memory
Base:
640KB
Ext:
28MB
↑/↓/←/→/<CR>/<Tab> to select or <PgUp>/<PgDn>/+/- to modify
<Esc> to return to main menu

5.4.2 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3), and memory disks when configured (Flash0, ROM0, RAM0, etc.). Figure 9 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy or two hard disks around, map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

A special field in this section entitled “Boot Method: (Windows CE/Boot Sector)” is used to configure the CE Ready feature of the BIOS. For normal booting (DOS, Windows NT, etc.), select “Boot Sector” or “Unused”.

5.4.2.1 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

5.4.3 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The following table shows the drive assignments for Ide0-Ide3:

Table 21. IDE0-IDE3 Drive Assignments

File System Name	Controller	Master/Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

User This type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is in common use.

Physical This type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC Cards.

LBA This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 16-Gbyte drives. *Use this method for all new drives.*

CHS This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translates the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or physical geometry might show data as being missing or corrupted.

5.5 Configuring Boot Actions

Embedded BIOS supports up to six different user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions can be used:

Drive A: - K: Boot operating system from specified drive. If “Loader” is set to “BootRecord” or “Unused”, then the standard boot record will be invoked, causing DOS, Windows 95/98, Windows NT, or other industry-standard operating systems to load. If “Boot Method” is set to “Windows CE”, then the boot drive’s boot record will not be used, and instead the BIOS will attempt to load and execute the Windows CE Kernel file, NK.BIN, from the root directory of each boot device.

Debugger Launch the Integrated BIOS Debugger. To return to the boot process from the debugger environment, type “G” at the debugger prompt and press ENTER.

MFGMODE Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connect to a host computer.

WindowsCE Execute a ROM-resident copy of Windows CE, if available. This feature is not applicable unless properly configured by the OEM in the BIOS adaptation.

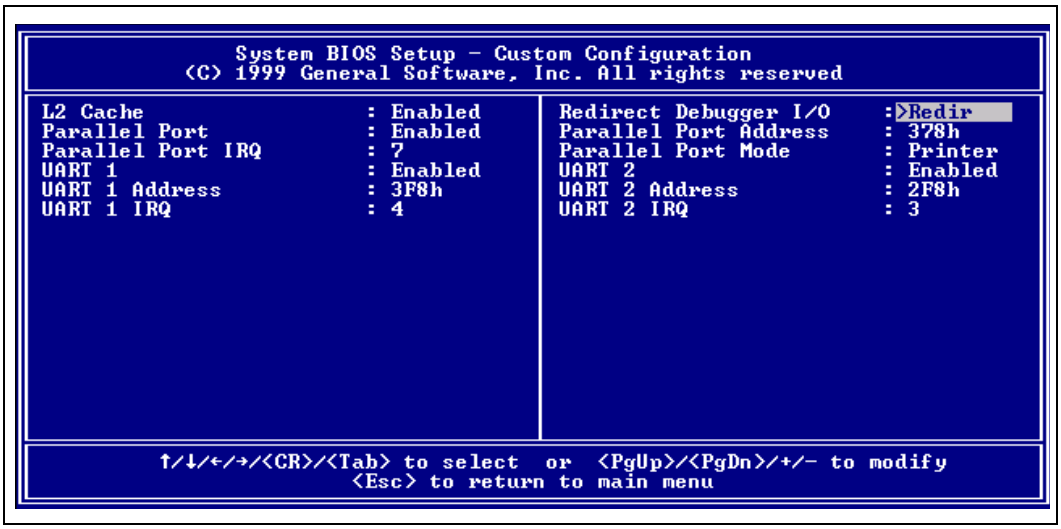
DOS in ROM Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS, such as Embedded DOS-ROM, has been stored in the BIOS boot ROM. Copies of Embedded DOS-ROM may be obtained from General Software.

None No action; POST proceeds to the next activity in the sequence.

5.6 Custom Configuration Setup Screen

The system’s hardware-specific features are configured with the Custom Setup Screen (Figure 10). All features are straightforward except for the Redirect Debugger I/O option, which is an extra embedded feature that allows the user to select whether the Integrated BIOS Debugger should use standard keyboard and video or RS232 console redirection for interaction with the user. If no video is available, the debugger is always redirected.

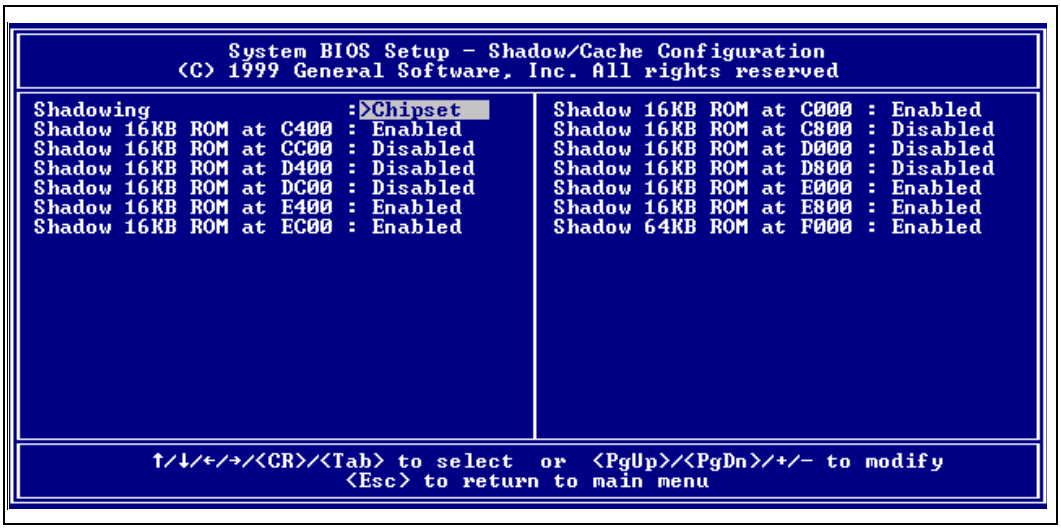
Figure 10. Embedded BIOS Custom Setup Screen


System BIOS Setup - Custom Configuration
(C) 1999 General Software, Inc. All rights reserved
L2 Cache : Enabled
Parallel Port : Enabled
Parallel Port IRQ : 7
UART 1 : Enabled
UART 1 Address : 3F8h
UART 1 IRQ : 4
Redirect Debugger I/O :>Redir
Parallel Port Address : 378h
Parallel Port Mode : Printer
UART 2 : Enabled
UART 2 Address : 2F8h
UART 2 IRQ : 3
↑/↓/←/→/<CR>/<Tab> to select or <PgUp>/<PgDn>/+/- to modify
<Esc> to return to main menu

5.7 Shadow Configuration Setup Screen

The system's Shadow Configuration Setup Screen (Figure 11) allows the selective enabling and disabling of shadowing in 16 Kbyte sections, except for the top 64 Kbytes of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance), and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 11. Embedded BIOS Shadow Setup Screen


System BIOS Setup - Shadow/Cache Configuration
(C) 1999 General Software, Inc. All rights reserved
Shadowing :>Chipset
Shadow 16KB ROM at C400 : Enabled
Shadow 16KB ROM at CC00 : Disabled
Shadow 16KB ROM at D400 : Disabled
Shadow 16KB ROM at DC00 : Disabled
Shadow 16KB ROM at E400 : Enabled
Shadow 16KB ROM at EC00 : Enabled
Shadow 16KB ROM at C000 : Enabled
Shadow 16KB ROM at C800 : Disabled
Shadow 16KB ROM at D000 : Disabled
Shadow 16KB ROM at D800 : Disabled
Shadow 16KB ROM at E000 : Enabled
Shadow 16KB ROM at E800 : Enabled
Shadow 64KB ROM at F000 : Enabled
↑/↓/←/→/<CR>/<Tab> to select or <PgUp>/<PgDn>/+/- to modify
<Esc> to return to main menu

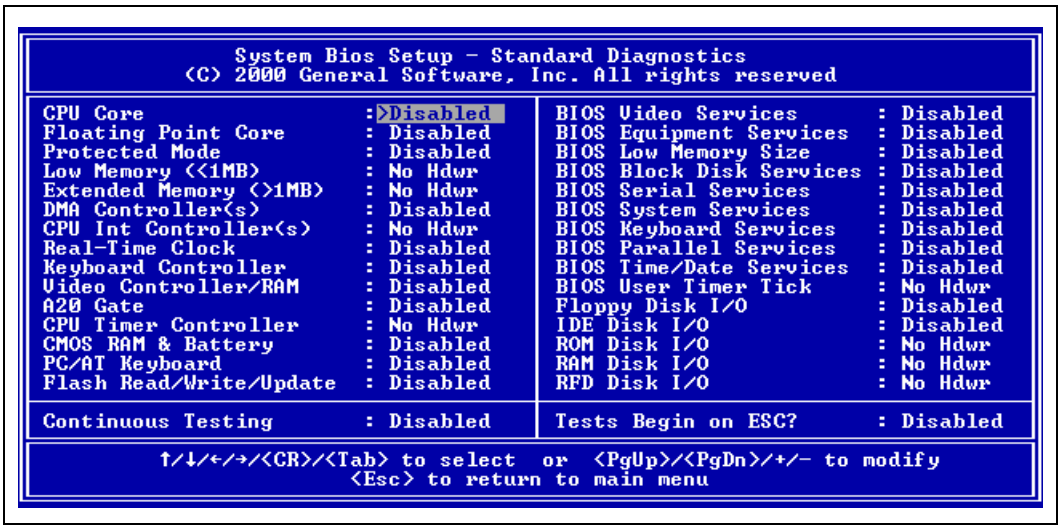
5.8 Standard Diagnostics Routines Setup Screen

Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 12). To use the system, selectively enable or disable features to be tested, and then enable the “Tests Begin on ESC?” option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the “Continuous Testing” option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used that do not contain data that could be harmed by the test.

Caution: The keyboard test may fail when the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 12. Standard Diagnostic Routines Setup Screen


System Bios Setup - Standard Diagnostics
(C) 2000 General Software, Inc. All rights reserved
CPU Core : >Disabled
Floating Point Core : Disabled
Protected Mode : Disabled
Low Memory (<1MB) : No Hdwr
Extended Memory (>1MB) : No Hdwr
DMA Controller(s) : Disabled
CPU Int Controller(s) : No Hdwr
Real-Time Clock : Disabled
Keyboard Controller : Disabled
Video Controller/RAM : Disabled
A20 Gate : Disabled
CPU Timer Controller : No Hdwr
CMOS RAM & Battery : Disabled
PC/AT Keyboard : Disabled
Flash Read/Write/Update : Disabled
BIOS Video Services : Disabled
BIOS Equipment Services : Disabled
BIOS Low Memory Size : Disabled
BIOS Block Disk Services : Disabled
BIOS Serial Services : Disabled
BIOS System Services : Disabled
BIOS Keyboard Services : Disabled
BIOS Parallel Services : Disabled
BIOS Time/Date Services : Disabled
BIOS User Timer Tick : No Hdwr
Floppy Disk I/O : Disabled
IDE Disk I/O : Disabled
ROM Disk I/O : No Hdwr
RAM Disk I/O : No Hdwr
RFD Disk I/O : No Hdwr
Continuous Testing : Disabled
Tests Begin on ESC? : Disabled
↑/↓/←/→/<CR>/<Tab> to select or <PgUp>/<PgDn>/+/- to modify
<Esc> to return to main menu

5.9 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EB43DBG:

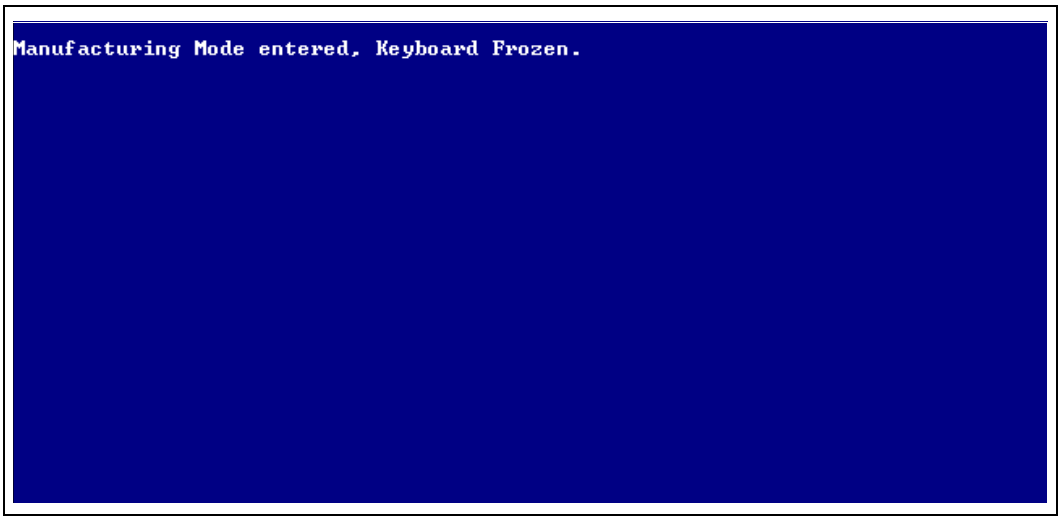
and await debugger commands. To return back to the Setup Screen main menu, type the following command, which instructs the debugger to “go”:

EB43DBG: **G** <ENTER>

5.10 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the console of the system (Figure 13). The host can resume operation of the system and give control back to the system Setup Screen system with special control software.

Figure 13. Start RS232 Manufacturing Link Setup Screen



5.11 Manufacturing Mode

The system's BIOS provides a special mode, called Manufacturing Mode, that allows the target to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the target's drives and manage the file systems on the target, reprogram flash memories, and test target hardware.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this chapter. Complete documentation and host-side software is available directly from General Software. For more information, visit the General Software Web site at http://www.gensw.com.

5.11.1 Console Redirection

The system can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with HYPERTERMINAL, see the debugger section's screen display (Figure 15).

To use the Console Redirection feature, remove the video display card from the system so that no video ROM is available for the BIOS to detect. In the absence of any video support, the BIOS automatically switches its keyboard and screen functions to serial I/O over COM1 on the board. The hardware connection to the host computer requires a null modem cable.

The software on the target can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to stall or not accept input.

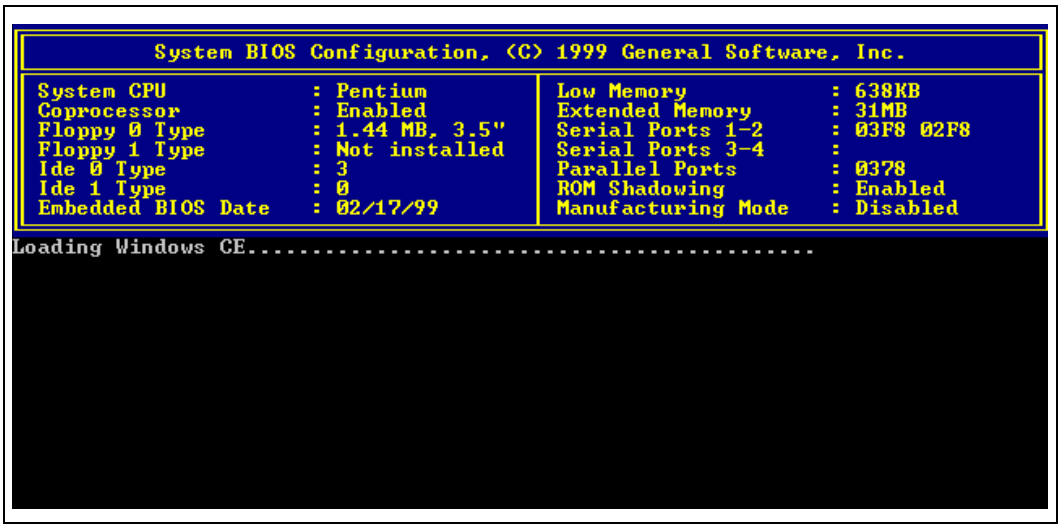
Caution: HYPERTERMINAL's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none", save the session, and exit HYPERTERMINAL. Then reinvoke HYPERTERMINAL with the session and it will operate with the new flow control setting.

5.11.2 CE-Ready Windows CE Loader

Your system's BIOS is CE-ready and can directly boot Windows CE without loading an intermediate operating system such as DOS and LOADCEPC. Instead, the NK.BIN file can be placed on a disk drive or drive emulator, and then the BIOS can be configured through the Basic CMOS Configuration Setup Screen to boot the NK.BIN file from the boot drives instead of the boot records on those drives.

To configure your system to boot Windows CE natively from a disk drive, set the "Boot Method" field to "Windows CE" in the Basic CMOS Configuration Setup Screen. Then, place a copy of NK.BIN suitable for execution by LOADCEPC in the root directory of your normal boot drive, such as drive C:. Then, reboot the system. The configuration box should be displayed (Figure 14), and immediately following should be the message "Loading Windows CE…" followed by a series of dots, indicating that the loading process is continuing. Once fully loaded, Windows CE takes over the system and runs using the standard PC keyboard, screen, and PS/2 mouse.

Figure 14. CE-Ready Boot Feature

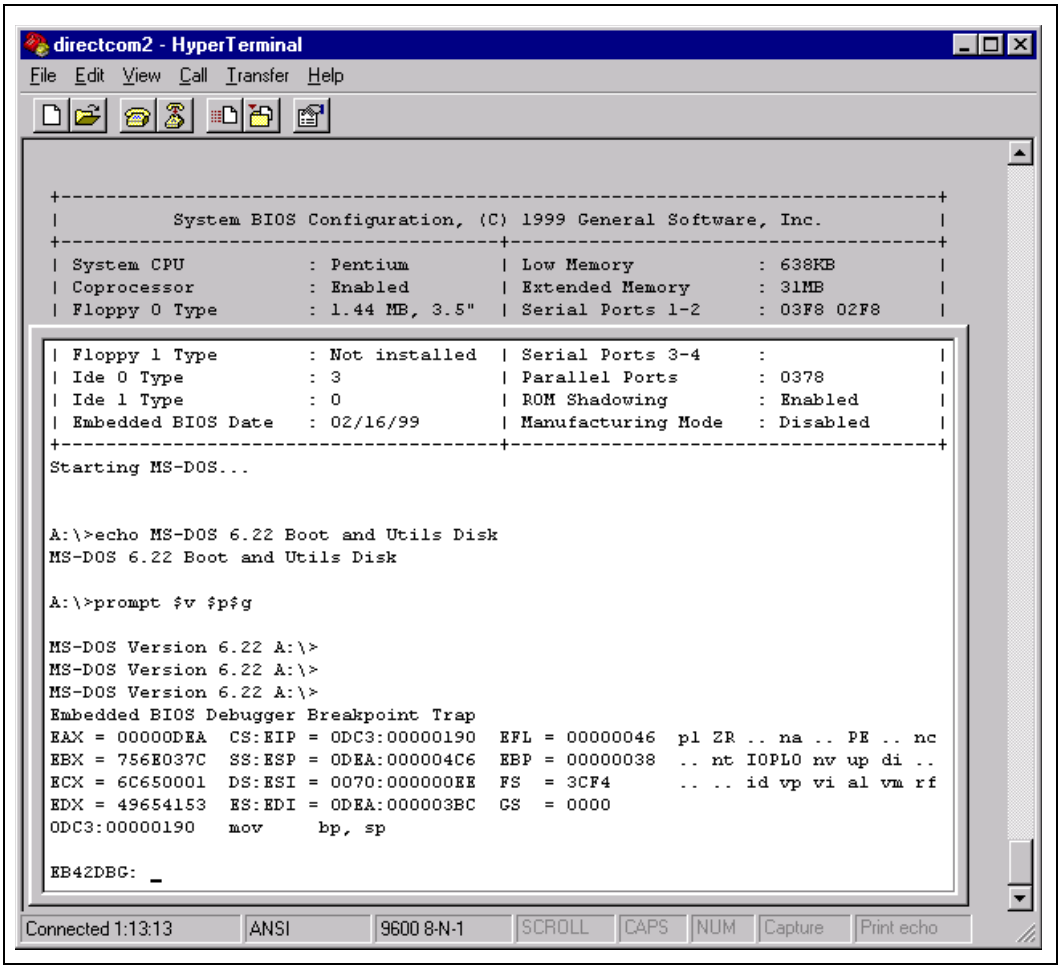

System BIOS Configuration, (C) 1999 General Software, Inc.
System CPU : Pentium
Coprocessor : Enabled
Floppy 0 Type : 1.44 MB, 3.5"
Floppy 1 Type : Not installed
Ide 0 Type : 3
Ide 1 Type : 0
Embedded BIOS Date : 02/17/99
Low Memory : 638KB
Extended Memory : 31MB
Serial Ports 1-2 : 03F8 02F8
Serial Ports 3-4 :
Parallel Ports : 0378
ROM Shadowing : Enabled
Manufacturing Mode : Disabled
Loading Windows CE.....

5.11.3 Integrated BIOS Debugger

The system's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the evaluation board. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see "Console Redirection" on page 58).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the HYPERTERMINAL session below (Figure 15) will appear, containing the title, “Embedded BIOS Debugger Breakpoint Trap” and a snapshot of the processor general registers.

Figure 15. Integrated BIOS Debugger Running Over a Remote Terminal


directcom2 - HyperTerminal
File Edit View Call Transfer Help
+--+
| System BIOS Configuration, (C) 1999 General Software, Inc. |
+--+--+
System CPU : Pentium	Low Memory : 638KB
Coprocessor : Enabled	Extended Memory : 31MB
Floppy 0 Type : 1.44 MB, 3.5"	Serial Ports 1-2 : 03F8 02F8
Floppy 1 Type : Not installed	Serial Ports 3-4 :
Ide 0 Type : 3	Parallel Ports : 0378
Ide 1 Type : 0	ROM Shadowing : Enabled
Embedded BIOS Date : 02/16/99	Manufacturing Mode : Disabled
+--+--+
Starting MS-DOS...
A:\>echo MS-DOS 6.22 Boot and Utils Disk
MS-DOS 6.22 Boot and Utils Disk
A:\>prompt $v pg
MS-DOS Version 6.22 A:\>
MS-DOS Version 6.22 A:\>
MS-DOS Version 6.22 A:\>
Embedded BIOS Debugger Breakpoint Trap
EAX = 00000DEA CS:EIP = 0DC3:00000190 EFL = 00000046 pl ZR .. na .. PE .. nc
EBX = 756E037C SS:ESP = 0DEA:000004C6 EBP = 00000038 .. nt IOPL0 nv up di ..
ECX = 6C650001 DS:ESI = 0070:000000EE FS = 3CF4 .. .. id vp vi al vm rf
EDX = 49654153 ES:EDI = 0DEA:000003BC GS = 0000
0DC3:00000190 mov bp, sp
EB42DBG: _
Connected 1:13:13
ANSI
9600 8-N-1
SCROLL
CAPS
NUM
Capture
Print echo

To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the “G” command (short for “go”) and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see “Basic CMOS Configuration Screen” on page 52), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software via the Web at http://www.gensw.com.

5.12 Embedded BIOS POST Codes

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80H during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored on the on-board Post Code Debugger located at U12 and U13. They are not displayed on the screen. For more information about POST codes, contact General Software.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START00h	Start	POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.
POST_STATUS_BOARD	13h	Initialize board, start memory bank detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US1	ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB1	bh	Test base 64 KB memory.
POST_STATUS_TESTDATA1	ch	Test data lines.
POST_STATUS_TESTADDR2	0h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO2	bh	Initialize before video ROM check.

```
POST_STATUS_VIDEOROM          2ch    Passing control to video ROM.
POST_STATUS_POSTVIDEO         2dh    Control returned from video ROM.
POST_STATUS_CHECKEGAVGA       2eh    Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY   2fh    No EGA/VGA found, test video memory.
POST_STATUS_RETRACE           30h    Scan for video retrace signal.
POST_STATUS_ALTDISPLAY        31h    Primary retrace failed.
POST_STATUS_ALTRETRACE        32h    Alternate found.
POST_STATUS_VRFYSWADAPTER     33h    Verify video switches.
POST_STATUS_SETDISPMODE       34h    Establish display mode.
POST_STATUS_CHECKSEG40A       35h    Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR         36h    Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY      37h    Display power-on message.
POST_STATUS_SAVECURSOR        38h    Save cursor position.
POST_STATUS_BIOSIDENT         39h    Display BIOS identification string.
POST_STATUS_HITDEL            3ah    Display "Hit <DEL> to ..." message.
POST_STATUS_VIRTUAL           40h    Prepare protected mode test.
POST_STATUS_DESCR             41h    Prepare descriptor tables.
POST_STATUS_ENTERVM           42h    Enter virtual mode for memory test.
POST_STATUS_ENABINT           43h    Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1        44h    Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2        45h    Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS      46h    Write extended memory test patterns.
POST_STATUS_LOWPATTERNS       47h    Write conventional memory test patterns.
POST_STATUS_FINDLOWMEM        48h    Find low memory size from patterns.
POST_STATUS_FINDHIMEM         49h    Find high memory size from patterns.
POST_STATUS_CHECKSEG40B       4ah    Verify ROM BIOS data area again.
POST_STATUS_CHECKDEL          4bh    Check for <DEL> pressed.
POST_STATUS_CLREXTMEM         4ch    Clear extended memory for soft reset.
POST_STATUS_SAVEMEMSIZE       4dh    Save memory size.
POST_STATUS_COLD64TEST        4eh    Cold boot: Display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST       4fh    Cold boot: Test all of low memory.
POST_STATUS_ADJUSTLOW         50h    Adjust memory size for EBDA usage.
POST_STATUS_COLDHITEST        51h    Cold boot: Test high memory.
POST_STATUS_REALMODETEST      52h    Prepare for shutdown to real mode.
POST_STATUS_ENTERREAL         53h    Return to real mode.
POST_STATUS_SHUTDOWN          54h    Shutdown successful.
POST_STATUS_DISABA20          55h    Disable A20 line.
POST_STATUS_CHECKSEG40C       56h    Check ROM BIOS data area again.
POST_STATUS_CHECKSEG40D       57h    Check ROM BIOS data area again.
POST_STATUS_CLRHITDEL         58h    Clear "Hit <DEL>" message.
POST_STATUS_TESTDMAPAGE       59h    Test DMA page register file.
POST_STATUS_VRFYDISPMEM       60h    Verify from display memory.
POST_STATUS_TESTDMA0BASE      61h    Test DMA0 base register.
POST_STATUS_TESTDMA1BASE      62h    Test DMA1 base register.
POST_STATUS_CHECKSEG40E       63h    Checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F       64h    Checking ROM BIOS data area again.
POST_STATUS_PROGDMA           65h    Program DMA controllers.
POST_STATUS_INITINTCTRL       66h    Initialize PICs.
POST_STATUS_STARTKBDTEST      67h    Start keyboard test.
POST_STATUS_KBDRESET          80h    Issue KB reset command.
POST_STATUS_CHECKSTUCKKEYS    81h    Check for stuck keys.
POST_STATUS_INITCIRCBUFFER    82h    Initialize circular buffer.
POST_STATUS_CHECKLOCKEDKEYS   83h    Check for locked keys.
POST_STATUS_MEMSIZEMISMATCH   84h    Check for memory size mismatch.
POST_STATUS_PASSWORD          85h    Check for password or bypass setup.
```

POST_STATUS_BEFORESETUP	86h	Password accepted.
POST_STATUS_CALLSETUP	87h	Entering setup system.
POST_STATUS_POSTSETUP	88h	Setup system exited.
POST_STATUS_DISPPWRON	89h	Display power-on screen message.
POST_STATUS_DISPWAIT	8ah	Display "Wait..." message.
POST_STATUS_ENABSHADOW	8bh	Shadow system & video BIOS.
POST_STATUS_STDCMOSSETUP	8ch	Load standard setup values from CMOS.
POST_STATUS_MOUSE	8dh	Test and initialize mouse.
POST_STATUS_FLOPPY	8eh	Test floppy disks.
POST_STATUS_CONFIGFLOPPY	8fh	Configure floppy drives.
POST_STATUS_IDE	90h	Test hard disks.
POST_STATUS_CONFIGIDE	91h	Configure IDE drives.
POST_STATUS_CHECKSEG40G	92h	Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H	93h	Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE	94h	Set base & extended memory sizes.
POST_STATUS_SIZEADJUST	95h	Adjust low memory size for EBDA.
POST_STATUS_INITC8000	96h	Initialize before calling C800h ROM.
POST_STATUS_CALLC8000	97h	Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000	98h	ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE	99h	Configure timer/printer data.
POST_STATUS_SERIALBASE	9ah	Configure serial port base addresses.
POST_STATUS_INITBEFORENPX	9bh	Prepare to initialize coprocessor.
POST_STATUS_INITNPX	9ch	Initialize numeric coprocessor.
POST_STATUS_POSTNPX	9dh	Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS	9eh	Check KB settings.
POST_STATUS_ISSUEKBDID	9fh	Issue keyboard ID command.
POST_STATUS_RESETID	0a0h	KB ID flag reset.
POST_STATUS_TESTCACHE	0a1h	Test cache memory.
POST_STATUS_DISPSOFTERR	0a2h	Display soft errors.
POST_STATUS_TYPEMATIC	0a3h	Set keyboard typematic rate.
POST_STATUS_MEMWAIT	0a4h	Program memory wait states.
POST_STATUS_CLRSCR	0a5h	Clear screen.
POST_STATUS_ENABPTYNMI	0a6h	Enable parity and NMIs.
POST_STATUS_INITE000	0a7h	Initialize before calling ROM at E000h.
POST_STATUS_CALLE000	0a8h	Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000	0a9h	ROM extension returned.
POST_STATUS_DISPCONFIG	0b0h	Display system configuration box.
POST_STATUS_INT19BOOT	00h	Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH	0b1h	Test low memory exhaustively.
POST_STATUS_EXTMEMEXH	0b2h	Test extended memory exhaustively.
POST_STATUS_PCIENUM	0b3h	Enumerate PCI busses.

5.13 Embedded BIOS Beep Codes

Embedded BIOS tests much of the system hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64 KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64 KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard tes t failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

Table 22. Bill of Materials (Sheet 1 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
U7	CHIPSET (GMCH)	INTEL	FW82815		
U15	CODEC	YAMAHA	YMF752-S		
U17	CHIPSET	WINBOND	W83627HF-AW "C"	WINBOND W83627HF-AW "D"	
U12	CHIPSET (ICH2)	INTEL	FW82801BA		
U11	LINEAR IC	NS	LM4880MX		
U19	TTL-74LVC06A	TI	74LVC06A	FAIRCHILD 74LCX06	
U18	TTL-74LVC07A	TI	74LVC07A	FAIRCHILD 74LCX07	
U20	TTL-74LCX14	FAIRCHILD	74LCX14	MOTOROLA 74LVC14	
U8	TTL-PI5C3384QX	PERICOM	PI5C3384QX	IDT 74FST3384Q, TI 74CBT3384A	
U5	TTL-PAC-SZ1284-02	CMD	PAC-SZ1284-02		
U28	TTL-PAC-VGA201	CMD	PAC-VGA201		
U9,U10	TTL-75232	GOLDSTAR	75232	TI GD75232, ALI M5232 PA1	
U6	CLOCK GENERATOR	ICS	ICS9250BF-28		
U29	CLOCK GENERATOR	ICS	ICS9112BM-17		
Q2,Q18	TRANSISTOR	FAIRCHILD	MMBT2907A	MOTOROLA MMBT2907A, PHILIPS PMBT2907A	
Q1,Q13,Q16,Q17	TRANSISTOR	PHILIPS	2N7002	VISHAY 2N7002E, FAIRCHILD 2N7002	

Table 22. Bill of Materials (Sheet 2 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
Q14,Q15,Q19,Q20,Q21,Q22	TRANSISTOR	PHILIPS	PMBS3904	FAIRCHILD MMBT3904, MOTOROLA MMBT3904	
Q5	TRANSISTOR	FAIRCHILD	NDS356AP		
Q4	TRANSISTOR	FAIRCHILD	NZT651		
U2	REGULATOR	RICHTEK	RT9641ACS		
Q3,Q24	REGULATOR	FAIRCHILD	RC1117ST	AMS AMS1117, AMI AME1117ACGT	
U4	REGULATOR	RICHTEK	RT9230CS		
Q10,Q12	MOSFET	FAIRCHILD	SSR3055LA	PHILIPS PHD3055E	
Q7,Q11	MOSFET	HARRIS	HUF76107D3S		
Q6,Q9	MOSFET	PHILIPS	PHB55N03LT		
Q8	MOSFET	FAIRCHILD	FDS8936A	FAIRCHILD NDS8936	
D1,D4,D5,D10,D13,D14,D15,D17	DIODE	VISHAY	LL4148-RF	VISHAY LL4148, PHILIPS BAS32L	
D2,D6,D7,D8,D12,D18	DIODE	WILLAS	SS12	MICROSEMI SS12	
D3	DIODE	MICROSEMI	SK32B		
PCI1,PCI2,PCI3	SLOT	MOLEX	120 PIN (PCI) 'NYLON"	FOXCONN 120 PIN (PCI), ATMEL 120 PIN (PCI)	
AGP1	SLOT	MOLEX	AGP 132PIN UNIVERSAL	FOXCONN AGP 132PIN UNIVERSAL, TEKCON AGP 132PIN UNIVERSAL	
Y3	X'TAL	H.ELE	14.318MHZ (VERTICAL)	FUJICOM 14.318MHZ (VERTICAL), TQG 14.318MHZ (VERTICAL)	
Y1	X'TAL	H.ELE	24.576MHZ(VERTICAL)	TQG 24.576MHZ(VERTICAL)	

Table 22. Bill of Materials (Sheet 3 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
Y2	X'TAL	KDS	32.768KHZ	EPSON 32.768KHZ, CITIZEN 32.768KHZ	
DIMM1,DIMM2,DIMM3	SOCKET	MOLEX	DIMM UNBUFFERED 168PIN 3.3V NYLON	FOXCONN DIMM UNBUFFERED 168PIN 3.3V, TEKCON DIMM UNBUFFERED 168PIN 3.3V NYLON	
U3	SOCKET	FOXCONN	370 PIN ZIF(ANTI-FLUX)NEW	AMP 370 PIN ZIF	
U23	SOCKET	FOXCONN	32 PIN		
SP1	BUZZER	HYPAK	KC-1206		
U7	HEAT SINK	AAVID	37.4*37.4*9.8mm +LATCH GREEN		
SW1	DIP SWITCH		8*2 PIN		
JP1(1-2)	JUMPER		2PIN (BLACK)		
BAT1	BATTERY SOCKET	LOTES			
D16	LED		RED		
S1,JP3	HEADER		2*1 PIN		
JP1	HEADER		3*1 PIN		
WOL1	HEADER		WAFER WOL 3*1PIN PITCH 2mm		
AUX1,CD2	HEADER		WAFER 4*1PIN(CD-IN)		
JP4	HEADER		5*1 PIN(CUT PIN1)		
IR1,SMB1,SMB2,JP5	HEADER		5*1 PIN		
USB2	HEADER		5*2 PIN CUT PIN 1,2		
COM2	HEADER		5*2 PIN		
PN1	HEADER		14x1 PIN w/ No. 6,9,12 MISSING		
PN2	HEADER		14x1 PIN w/ No. 3,8,11 MISSING		
FDC1	HEADER		WAFER 17*2 PIN		
VL1	HEADER		20*2PIN(F)		

Table 22. Bill of Materials (Sheet 4 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
IDE1,IDE2	HEADER		WAFER 20*2PIN CUT PIN20(?)		
FAN1,FAN2,FAN3	HEADER	MOLEX	WAFER W/LOCK 3P		
ATXPR1	CON.	WIESON	MINI FIT CON.20PIN	TEKCON MINI FIT CON.20PIN(NEW)	
USB1	CON.	FOXCONN	USB CON. 2*4 PIN DUAL PORT	MOLEX USB CON. 2*4 PIN DUAL PORT(NEW), WIESON USB CON. 2*4 PIN DUAL PORT	
U1	KEYBOARD & MOUSE	WIESON	MINI-DIN 6Px2 DUAL PORT-PC99	FOXCONN MINI-DIN 6Px2 DUAL PORT-PC99	
CD1	CON.		WAFER 2.0m/m 4P		
CNRSLOT1	SLOT	FOXCONN	60 PIN (CNR)	MOLEX 60 PIN (CNR), AMP 60 PIN (CNR)	
JK1+JK2+JK3+J1	D-TYPE	FOXCONN	D-SUB 90° 15P(F)7+8/ PHONE*3-PC99		
VGA1	D-TYPE	FOXCONN	D-SUB 15PIN (F) 3*5(S)-PC99	TEKCON D-SUB 15PIN (F) 3*5(S)-PC99	
LPT1	D-TYPE	WIESON	D-SUB 90° 25PIN (F) RISE HIGH -PC99	TEKCON D-SUB 90° 25PIN (F) RISE HIGH -PC99	
COM1	D-TYPE	FOXCONN	D-SUB 9PIN (MALE) -PC99	WIESON D-SUB 9PIN (MALE) -PC99, TEKCON D-SUB 9PIN (MALE) -PC99	
BAT1	BATTERY	MAXELL	CR2032	PANASONIC CR2032, SONY CR2032	
RN74	R.P		0 OHM (8P 4R) - CONCAVE	0 OHM (8P 4R) - CONVEX	
RN36,RN37,RN38	R.P		10 OHM (8P 4R) - CONCAVE	10 OHM (8P 4R) - CONVEX	
RN70,RN71	R.P		15 OHM (8P 4R) - CONCAVE	15 OHM (8P 4R) - CONVEX	

Table 22. Bill of Materials (Sheet 5 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
RN19,RN20,RN69	R.P		22 OHM (8P 4R) - CONCAVE	22 OHM (8P 4R) - CONVEX	
RN34	R.P		33 OHM (8P 4R) - CONCAVE	33 OHM (8P 4R) - CONVEX	
RN3,RN5,RN6,RN7,RN8,RN9,RN10,	R.P		56 OHM (8P 4R) - CONCAVE	56 OHM (8P 4R) - CONVEX	
RN11,RN12,RN13,RN14,RN15,RN16,RN17,RN18,RN21,RN22,RN23,RN24,RN25,RN26,RN27,RN28,RN29,RN30,RN31,RN32,RN33	R.P				
RN39,RN40	R.P		1K (8P 4R) - CONCAVE	1K (8P 4R) - CONVEX	
RN41,RN59	R.P		2.2K (8P 4R) - CONCAVE	2.2K (8P 4R) - CONVEX	
RN58,RN64,RN66	R.P		2.7K (8P 4R) - CONCAVE	2.7K (8P 4R) - CONVEX	
RP2	R.P		2.7K (10P 8R) - CONVEX (3216)-R		
RN4,RN60	R.P		4.7K (8P 4R) - CONCAVE	4.7K (8P 4R) - CONVEX	
RN42,RN43,RN44,RN45,RN46,RN48,	R.P		8.2K (8P 4R) - CONCAVE		
RN49,RN51,RN54,RN55,RN75,RN77	R.P		8.2K (8P 4R) - CONVEX		
RN72,RN73	R.P		15K (8P 4R) - CONCAVE	15K (8P 4R) - CONVEX	
R37,R38,R40,R166,R207,R237,R240, R256,R315,R326,R327	RESISTOR		0 OHM (0603)		
R36,R47,R48,R52,R60, R72,R141,R321, R322	RESISTOR		10 OHM (0603)		
R44,R50,R51,R62,R63, R104,R105,R251, R275	RESISTOR		22 OHM (0603)		
R45,R46,R49,R57,R58, R64,R65,R66, R67,R85,R87,R112,R113,R191,R236, R277,R290,R320	RESISTOR		33 OHM (0603)		
R91,R98,R316,R317	RESISTOR		47 OHM (0603)		
R59	RESISTOR		51 OHM (0603)		
R23	RESISTOR		56 OHM (0603)		
R231,R232	RESISTOR		68 OHM (0603)		

Table 22. Bill of Materials (Sheet 6 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
R133,R142,R148,R154, R187,R230,R245	RESISTOR		100 OHM (0603)		
R1,R2,R5,R6,R7,R12,R 14,R15,R234,R243	RESISTOR		150 OHM (0603)		
R86,R238,R242	RESISTOR		220 OHM (0603)		
R185,R193	RESISTOR		300 OHM (0603)		
R8,R13,R199,R239	RESISTOR		330 OHM (0603)		
R16,R216	RESISTOR		510 OHM (0603)		
R9	RESISTOR		680 OHM (0603)		
R3,R4,R10,R19,R53,R 73,R84,R100, R115,R116,R117,R120, R121,R122,R129, R134,R181,R188,R196, R197,R198,R212, R217,R252,R254,R314, R323,R324,R325, R336	RESISTOR		1K (0603)		
R153	RESISTOR		1.8K (0603)		
R28,R106,R108,R110, R119,R226,R246, R328,R329	RESISTOR		2.2K (0603)		
R29	RESISTOR		3.9K (0603)		
R11,R54,R76,R79,R92, R93,R94,R95,R96, R97,R99,R101,R102,R 189,R218,R229	RESISTOR		4.7K (0603)		
R75,R83,R88,R89,R90, R206,R211,R249, R260,R261,R262,R263, R276,R332-R335	RESISTOR		8.2K (0603)		
R20,R70,R80,R107,R1 09,R147,R152, R157,R167,R208,R209, R214,R223,R233, R235,R241,R244,R255, R302,R303	RESISTOR		10K (0603)		
R174,R190,R272,R273	RESISTOR		15K (0603)		
R43,R126,R127,R128, R132,R247	RESISTOR		20K (0603)		
R210	RESISTOR		30K (0603)		
R192	RESISTOR		33K (0603)		
R118,R124,R125,R155, R337	RESISTOR		220K (0603)		
R266,R267	RESISTOR		330K (0603)		
R164,R271	RESISTOR		560K (0603)		

Table 22. Bill of Materials (Sheet 7 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
R149,R162,R213	RESISTOR		10M (0603)		
PR14	RESISTOR		15 OHM (1%) 0603		
R31	RESISTOR		22 OHM (1%) 0603		
R56	RESISTOR		33 OHM (1%)0603		
PR9,PR15,PR18,PR27	RESISTOR		40.2 OHM (1%)0603		
PR41	RESISTOR		60.4 OHM (1%)0603		
PR7,PR10,PR11,PR12, PR42	RESISTOR		75 OHM (1%)0603		
PR21,PR24	RESISTOR		82 OHM (1%)0603		
R33,R61	RESISTOR		90.9 OHM (1%)0603		
PR2,PR3	RESISTOR		100 OHM (1%) 0603		
PR1,PR5	RESISTOR		110 OHM 1% 0603		
PR40	RESISTOR		120 OHM (1%)0603		
PR4,PR6,PR8,PR43	RESISTOR		150 OHM (1%)0603		
PR13	RESISTOR		174 OHM (1%)0603		
PR19	RESISTOR		200 OHM (1%)0603		
R318,R319	RESISTOR		243 OHM 1% (0603)		
PR16,PR17,PR20,PR25,PR26	RESISTOR		301 OHM 1% (0603)		
PR22,PR23,R32,R55	RESISTOR		1K 1%(0603)		
R39	RESISTOR		1.43K (1%)0603		
PR36,PR38,PR39	RESISTOR		10K (1%)0603		
PR37	RESISTOR		28K (1%)0603		
PR33,PR35,R42	RESISTOR		56K(1%)0603		
PR32	RESISTOR		120K 1%(0603)		
PR34	RESISTOR		232K 1% (0603)		

Table 22. Bill of Materials (Sheet 8 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
RT1	THERMISTOR	SEMITEC	10K OHM ±3% (0603)		
C11,C14,C26,C60,C64, C67,C71	CAPACITOR		0.001UF (0603)		
BC26,BC28,BC29,BC32,BC33, BC46-BC48,BC51,BC52,BC55,BC57, BC59,BC62,BC63,BC65,BC74,BC75, BC79,BC80,BC82,BC87,BC88, BC90-BC98,BC105,BC114,BC119, BC124,BC144, BC147,BC149,BC150, BC158-BC160,BC169-BC171, BC181-BC183,BC186,BC187,BC222, BC226,C17,C85	CAPACITOR		0.01UF (0603)		
C4,C7,C27,C119,BC1-BC3,BC5, BC7-BC25,BC27,BC30,BC31, BC34-BC45,BC49,BC50,BC53,BC54, BC56,BC58,BC60,BC61,BC64,BC66, BC67,BC69-BC73,BC76-BC78,BC81, BC83-BC86,BC89,BC99-BC104, BC106-BC113,BC115,BC116, BC121-BC123,BC125,BC128, BC129,BC131,BC132,BC136, BC138-BC140,BC142,BC143,BC145, BC146,BC151,BC154-BC157,BC161-BC165,BC167, BC168,BC172,BC173,BC175, BC177-BC180,BC184,BC185,BC197, BC204-BC218,BC221,BC227, MC51, MC52,MC55	CAPACITOR		0.1UF (0603)		
BC68,BC223,BC224,BC225	CAPACITOR		0.22UF (0603)		
C110	CAPACITOR		0.047UF (0603)		

Table 22. Bill of Materials (Sheet 9 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
MC36,MC37,MC38,MC39,MC40,MC41, MC42,MC43,MC44,MC45,MC47,MC53, MC54,MC56,C5,C8,C13,C15,C18,C91, C104,C113	CAPACITOR		1UF (0603)		
MC48,MC57,MC59,C1, C2,C115	CAPACITOR		2.2UF (0805)		
MC1-MC6,MC8-MC10,MC13-MC15	CAPACITOR		4.7UF(1206)"X7R"		
MC7,MC11,MC12,MC16,MC17,MC18, MC19,MC20,MC21,MC22,MC23,MC24, MC25,MC26,MC27,MC28,MC29,MC30, MC31,MC32,MC33,MC34,MC35,MC46, MC60,MC61,MC62,MC63,MC66	CAPACITOR		4.7UF(1206)"Y5V		
C43,C47,C50	CAPACITOR		3.3PF(0603)		
C12,C16,C48,C53,C54, C56,C58,C99, C101	CAPACITOR		10PF (0603)		
C61	CAPACITOR		15PF (0603)		
C33,C35,C102,C103	CAPACITOR		18PF (0603)		
C36,C55,C57,C63,C65, C66,C68,C97,C98	CAPACITOR		22PF (0603)		
C44,C51,C125,C126	CAPACITOR		47PF (0603)		
C74,C75,C76,C79,C80, C81,C82,C83, C84,C86,C87,C90	CAPACITOR		100PF (0603)		
C59,C62,C70,C73,C122,BC4	CAPACITOR		470PF (0603)		
C69,C72	CAPACITOR		560PF (0603)		
C94,C95	CAPACITOR		2700PF (0603)		
C118	CAPACITOR		3300PF (0603)		
CN2,CN3,CN9,CN11	C/P		100PF (8P 4C) (1206)		
CP1,CP2,CP3,CP4	C/P		47PF(8P4C)(1206)		
CN1,CN8,CN10	C/P		470PF (8P 4C) (1206)		
EC6,EC11,EC20,EC40, EC41	E/C	TAYEH	10UF/25V (4*7)	JACKCON 10UF/25V (4*7)	

Table 22. Bill of Materials (Sheet 10 of 10)

Rev. 1.1

Reference Designator	Description	Manufacturer	Manuf. Part Number	Alternate Manufacturing Info	All Changes
EC3,EC26,EC27,EC28, EC33,EC35,EC36,	E/C	TAYEH	22UF/16V (4*7)	JACKCON 22UF/16V (4*7)	
EC5,EC10,EC15,EC17, EC18,EC19, EC22,EC30,EC39,C77, C78	E/C	TAYEH	100UF/16V (6.3*7)	JACKCON 100UF/16V (6*7)	
C6	T/C	SPRAGUE	33UF/20V "D"		
EC1,EC2,EC4,EC7,EC 8,EC9,EC12,EC13, EC14,EC21,EC23,EC2 4,EC25,EC29, EC31,EC32,EC34,C32	E/C E/C E/C	TAYEH JACKCON JPCON	1500UF/ 6.3V(8*16) 1500UF/ 6.3V(8*16) 1500UF/6.3V (8*16)		
L3	INDUCTOR	GLOMAG	IRON COIL 1UH(50MB)		
L1	INDUCTOR	GLOMAG	IRON COIL 2.5UH(5052)		
L2	INDUCTOR	MURATA	4.7UH (0805)		
L4	INDUCTOR	GLOMAG	IRON COIL 7UH(5052B)		
F1,F2,F4,F5,F6,F7	FUSE	BOURNS	POLY S/W MSMC110-2	RAYCHEM POLY S/ WSMDC100	
FB1,FB2,FB3,FB4,FB5, FB6,FB8,FB11, FB12,FB13,FB14,FB15, FB16,FB17, FB19-FB29	INDUCTOR	TAIYO	BEAD 241/ 100MHZ (0805) LL241	EMC BEAD 221/100MHZ (0805)	
VFB1,VFB2,VFB3,PFB 1,PFB2,PFB4, PFB5,PFB6,PFB11,PF B12,	INDUCTOR	MURATA	BEAD BLM11B750SPT(0603)		
U23	CHIPSET (FWH)	INTEL	N82802AC8		

Table 23. Key Components Bill of Materials

Rev. 1.1

Description	Manufacturer	Part #
815E Scalable Performance Board Development Kit Baseboard	ABIT	EIAP3815EDEVKIT
Intel® Pentium® III Processor at 866 MHz with 256K L2	Intel	RB80526PY866256
Intel® Celeron™ Processor at 850 MHz with 128K L2	Intel	RB80526RY850128
Thermal Solution	Agilent Technologies	Arcti-Cooler, HACA-0001
133 MHz, 128 Mbyte, SDRAM DIMM	SpecTek	P16M648YLDC9-133CL3A
Firmware Hub BIOS Memory, PLCC32 (8 Mbit)	Intel	N82802AC8
15.3 Gbyte Hard disk drive	Western Digital	WD153AA
BlueCat Linux OS Software (pre-installed on HDD)	LynuxWorks	N/A
Tornado 2.0/VxWorks CD	Wind River Systems	TEV-13720-ZC-00
ABIT SL-30 device driver CD	ABIT	SA-1.00E
Intel® Pro/100+ Management Adapter (Fast Ethernet Controller)	Intel	PILA8460B

NOTE: *This BOM does not include items such as mounting hardware, packaging material, documentation, etc.

Schematics B

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's Web site in PDF format.

- Block diagram
- PGA370 Part 1 and 2
- AGTL Termination
- Clock Synthesizer
- GMCH Part 1 and 2
- DIMM 1 and 2
- DIMM 3
- AGP
- ICH Part 1 and 2
- PCI 1 and 2
- PCI 3
- Video Bus & Connector
- FWH & UDMA100 IDE 1-2
- USB 0-3
- AC97 CODEC
- Audio I/O
- LPC I/O Controller & FDCL
- WOR, WOL & 2S1P
- KB, MS, GAME, & IR
- Front Panel & CNR
- ATX Power & H/W Monitor
- Voltage Regulator Part 1
- Voltage Regulator Part 2
- System Configuration
- PU/PDR and unused gates
- Decoupling capacitors

INTEL(R) PENTIUM(R) III & CELERON(TM) PROCESSOR(PPGA)/815E CHIPSET UNIPROCESSOR ABIT SCHEMATICS

REVISION 0.12

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DIMM 1 & 2	9
DIMM 3	10
AGP	11
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FWH & UDMA100 IDE 1-2	18
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AC97 CODEC	20
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LPC I/O CONTROLLER & FDCL	22
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ABIT SL30

**PLEASE NOTE THESE SCHEMATICS ARE SUBJECT TO CHANGE

ABIT Computer Corp.

Title: COVER SHEET		
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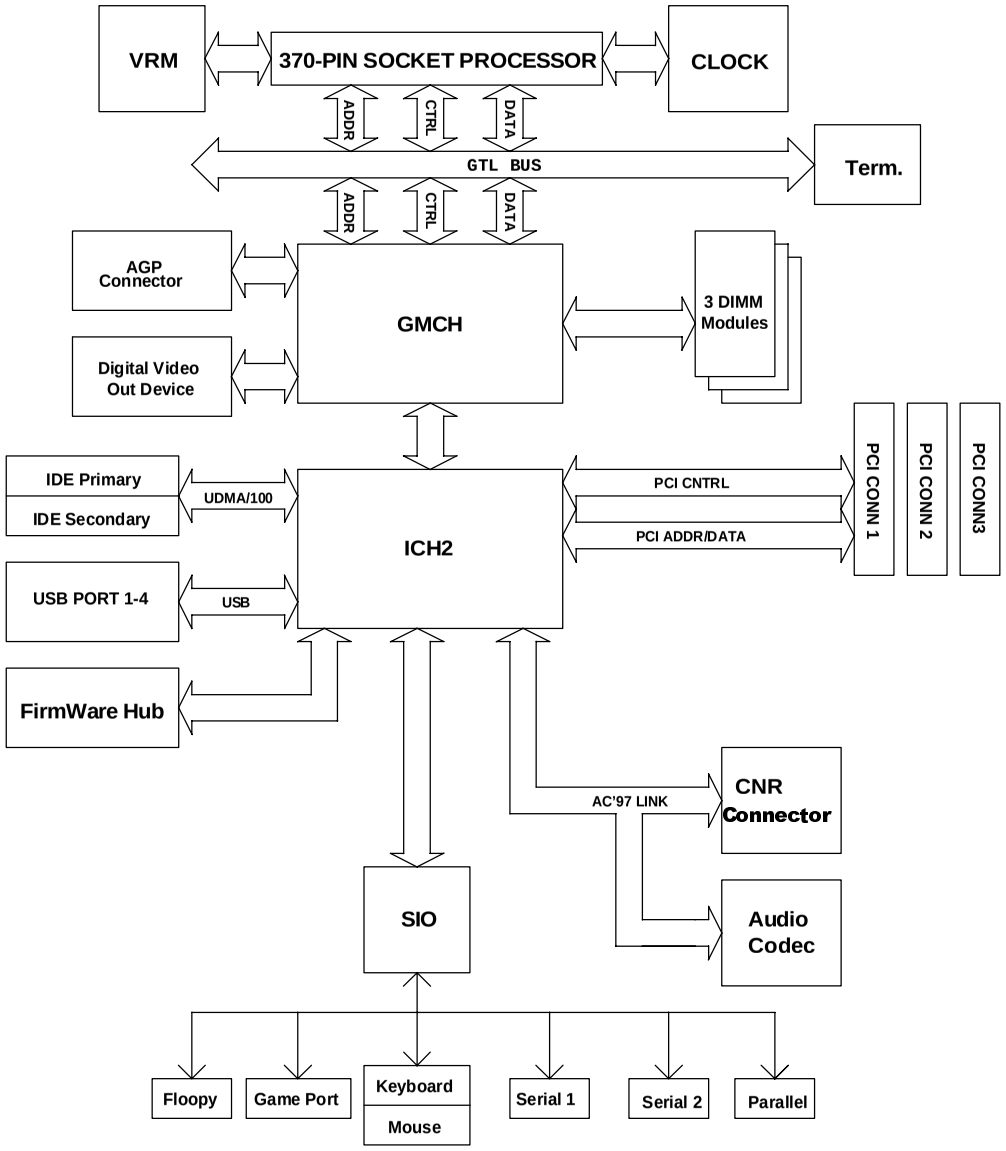
BLOCK DIAGRAM



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ABIT Computer Corp.

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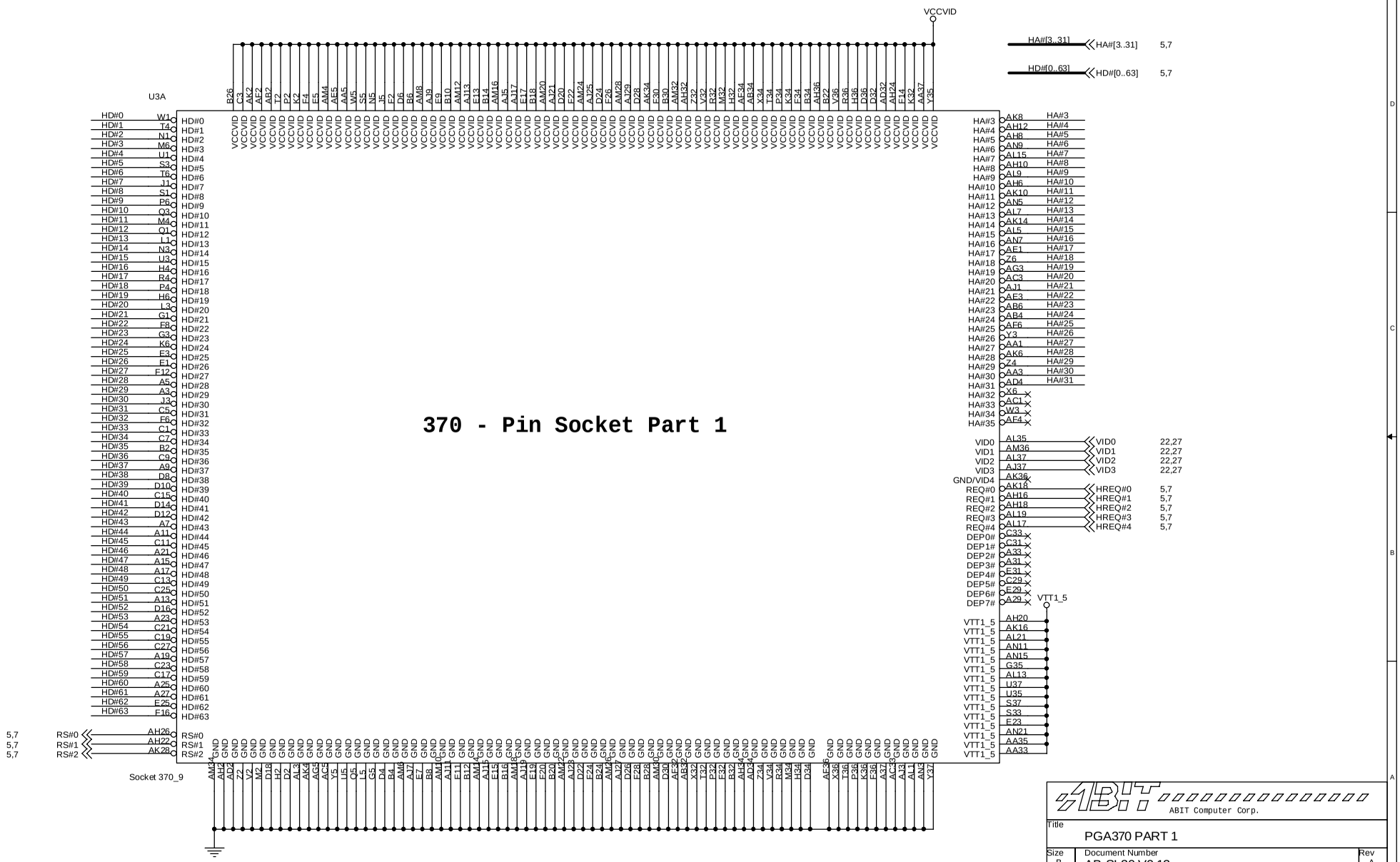

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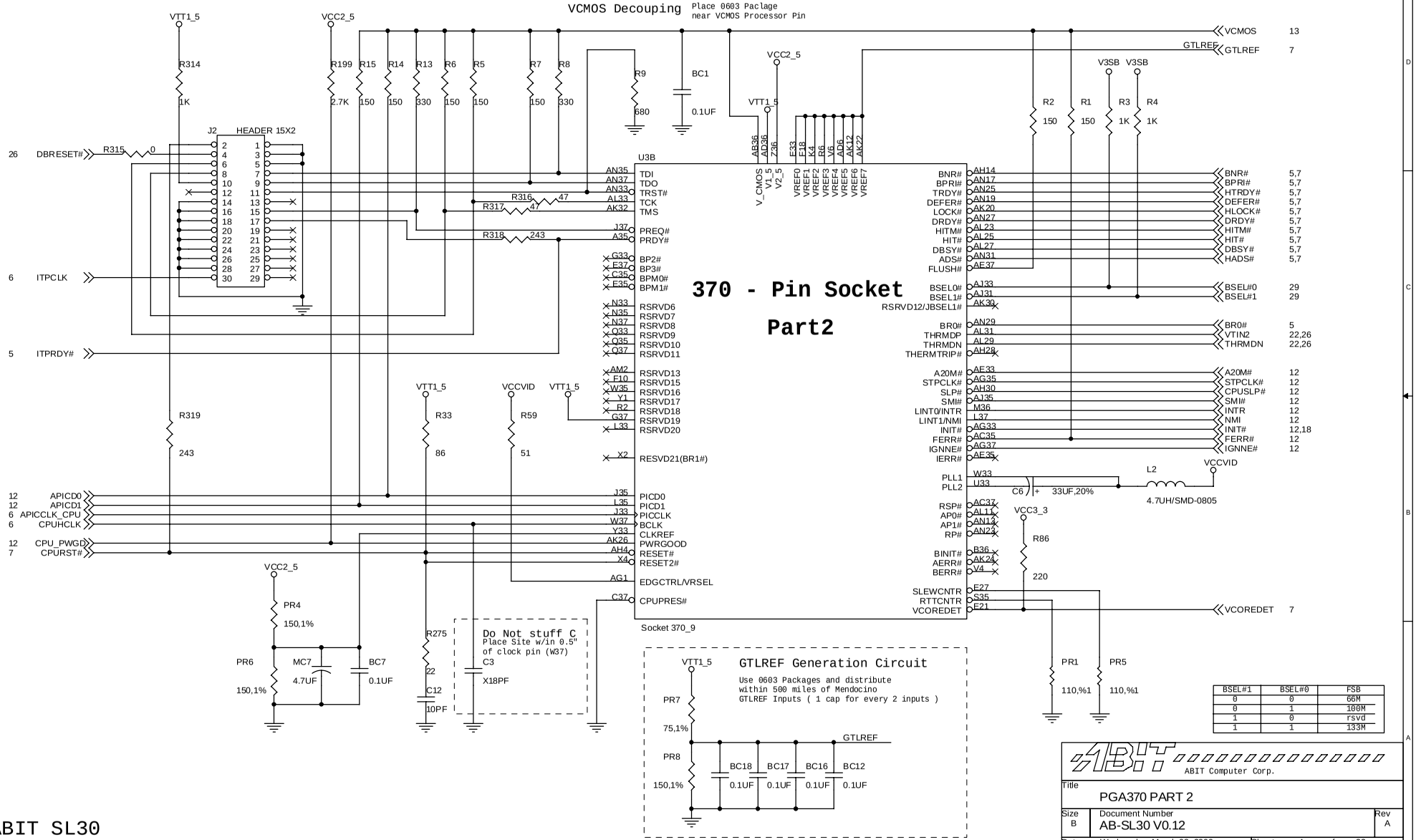

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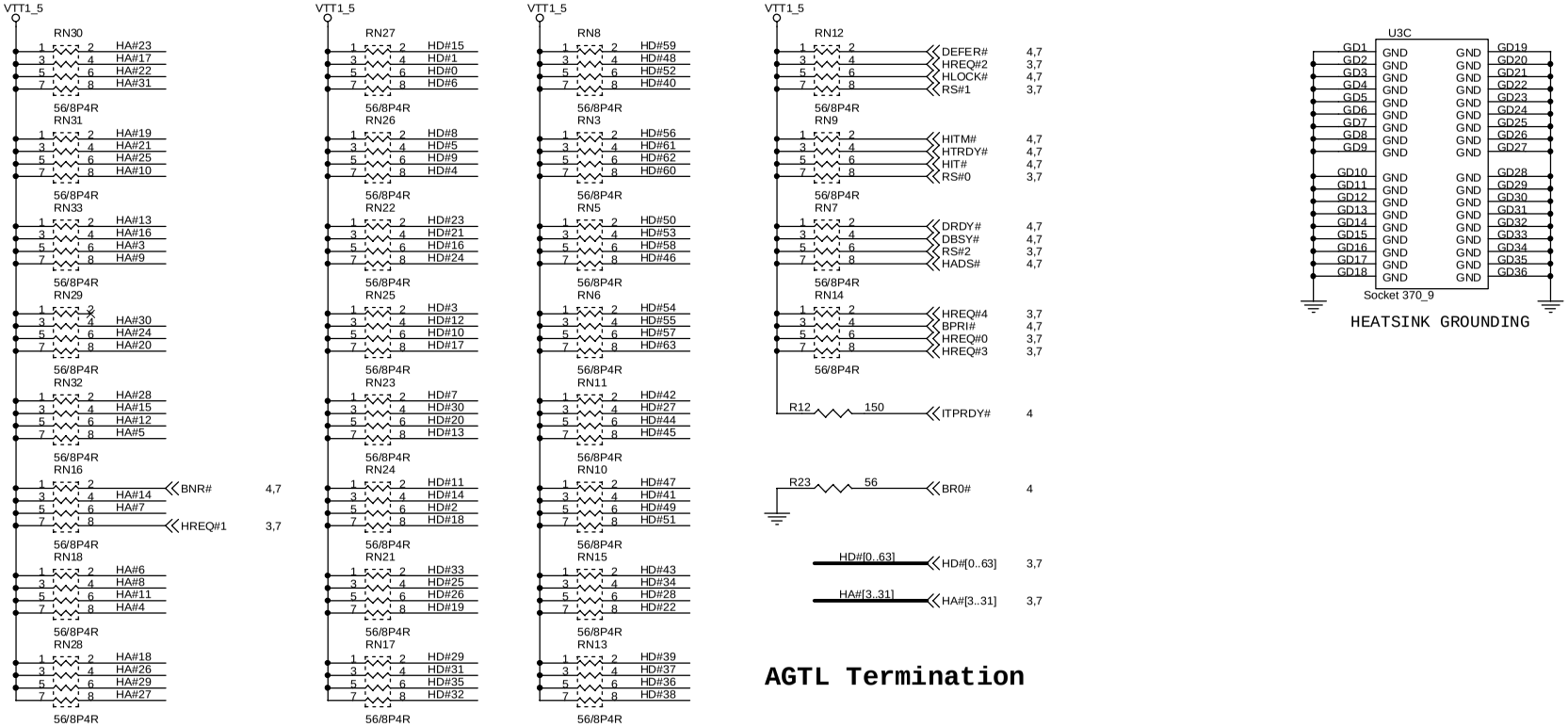

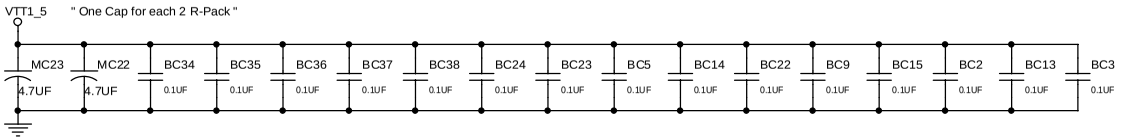

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Title	AGTL TERMINATION		
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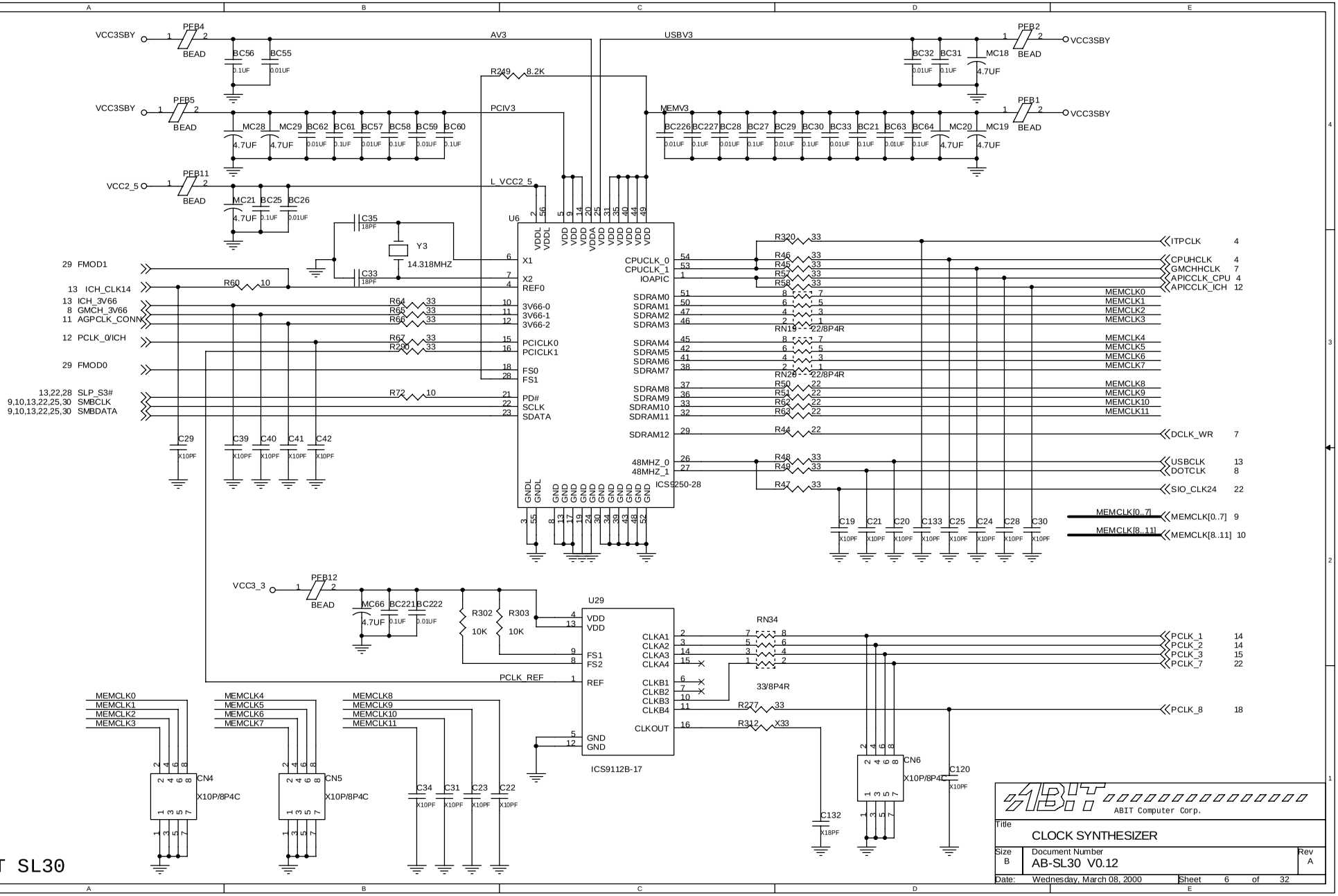
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BEAD
BC56
BC55
AV3
USBV3
PEB2
BC32
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MC18
R249 8.2K
PEB5
PCIV3
MEMV3
BC226
BC227
BC28
BC27
BC29
BC30
BC33
BC21
BC63
BC64
MC20
MC19
PEB1
MC28
MC29
BC62
BC61
BC57
BC58
BC59
BC60
VCC2_5
PEB11
L_VCC2_5
MC21
BC25
BC26
U6
C35
18PF
Y3
14.318MHZ
C33
29 FMOD1
13 ICH_CLK14
R60 10
13 ICH_3V66
8 GMCH_3V66
11 AGPCLK_CONN
12 PCLK_0/ICH
29 FMOD0
13,22,28 SLP_S3#
9,10,13,22,25,30 SMBCLK
9,10,13,22,25,30 SMBDATA
R64 33
R65 33
R66 33
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X2
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GNDL
GND
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CPUCLK_1
IOAPIC
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SDRAM1
SDRAM2
SDRAM3
SDRAM4
SDRAM5
SDRAM6
SDRAM7
SDRAM8
SDRAM9
SDRAM10
SDRAM11
SDRAM12
48MHZ_0
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R320 33
R46 33
R45 33
R57 33
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R50 22
R51 22
R62 22
R63 22
R44 22
R48 33
R49 33
R47 33
ITPCLK 4
CPUHCLK 4
GMCHHCLK 7
APICCLK_CPU 4
APICCLK_ICH 12
MEMCLK0
MEMCLK1
MEMCLK2
MEMCLK3
MEMCLK4
MEMCLK5
MEMCLK6
MEMCLK7
MEMCLK8
MEMCLK9
MEMCLK10
MEMCLK11
DCLK_WR 7
USBCLK 13
DOTCLK 8
SIO_CLK24 22
MEMCLK[0..7]
MEMCLK[0..7] 9
MEMCLK[8..11]
MEMCLK[8..11] 10
C29
C39
C40
C41
C42
C19
C21
C20
C133
C25
C24
C28
C30
X10PF
VCC3_3
PEB12
MC66
BC221
BC222
4.7UF
R302 10K
R303 10K
U29
VDD
FS1
FS2
REF
PCLK_REF
CLKA1
CLKA2
CLKA3
CLKA4
CLKB1
CLKB2
CLKB3
CLKB4
CLKOUT
GND
ICS9112B-17
RN34
33/8P4R
R277 33
R312 X33
PCLK_1 14
PCLK_2 14
PCLK_3 15
PCLK_7 22
PCLK_8 18
CN4
CN5
CN6
X10P/8P4C
C34
C31
C23
C22
C120
C132
X18PF
ABIT SL30
ABIT Computer Corp.
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Size
B
Document Number
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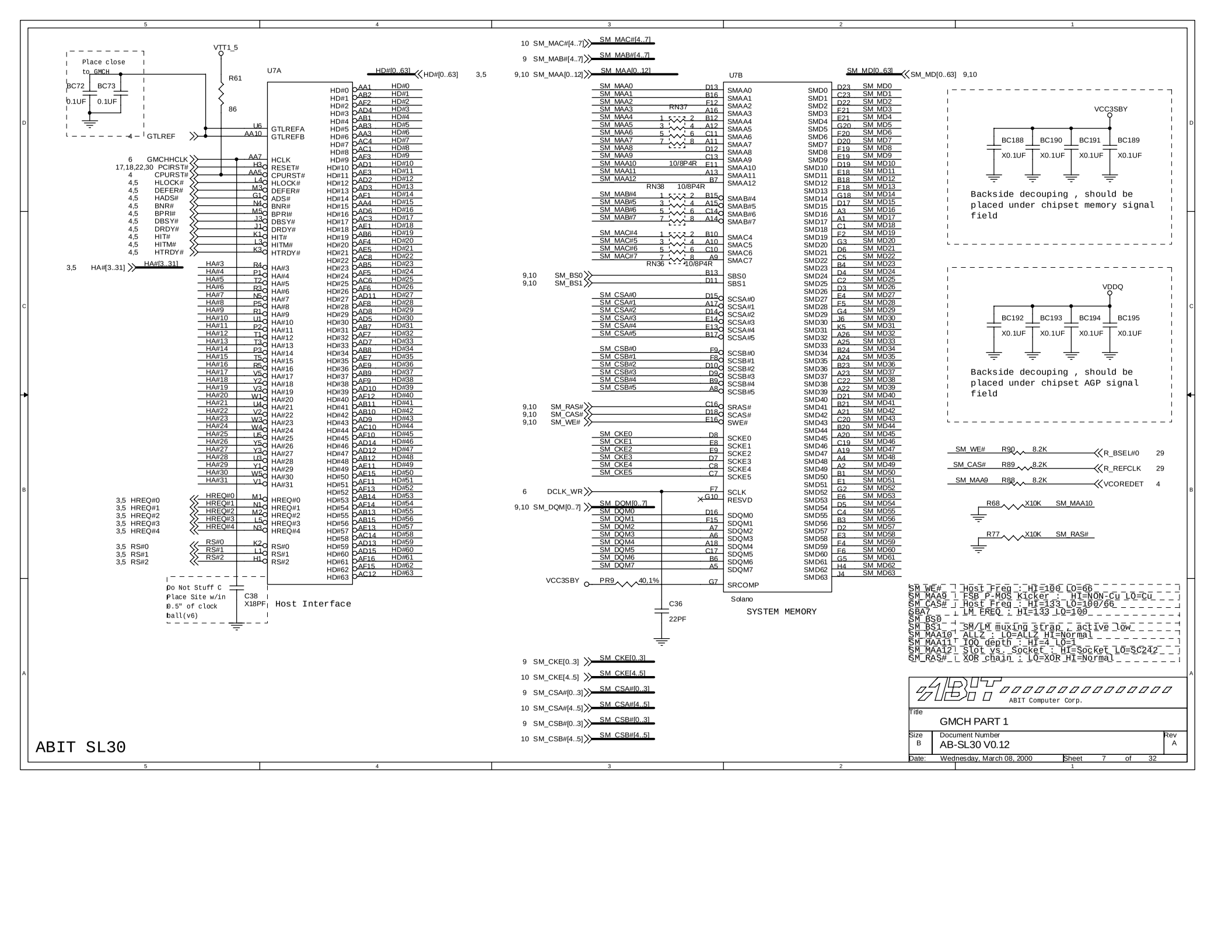
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U7A
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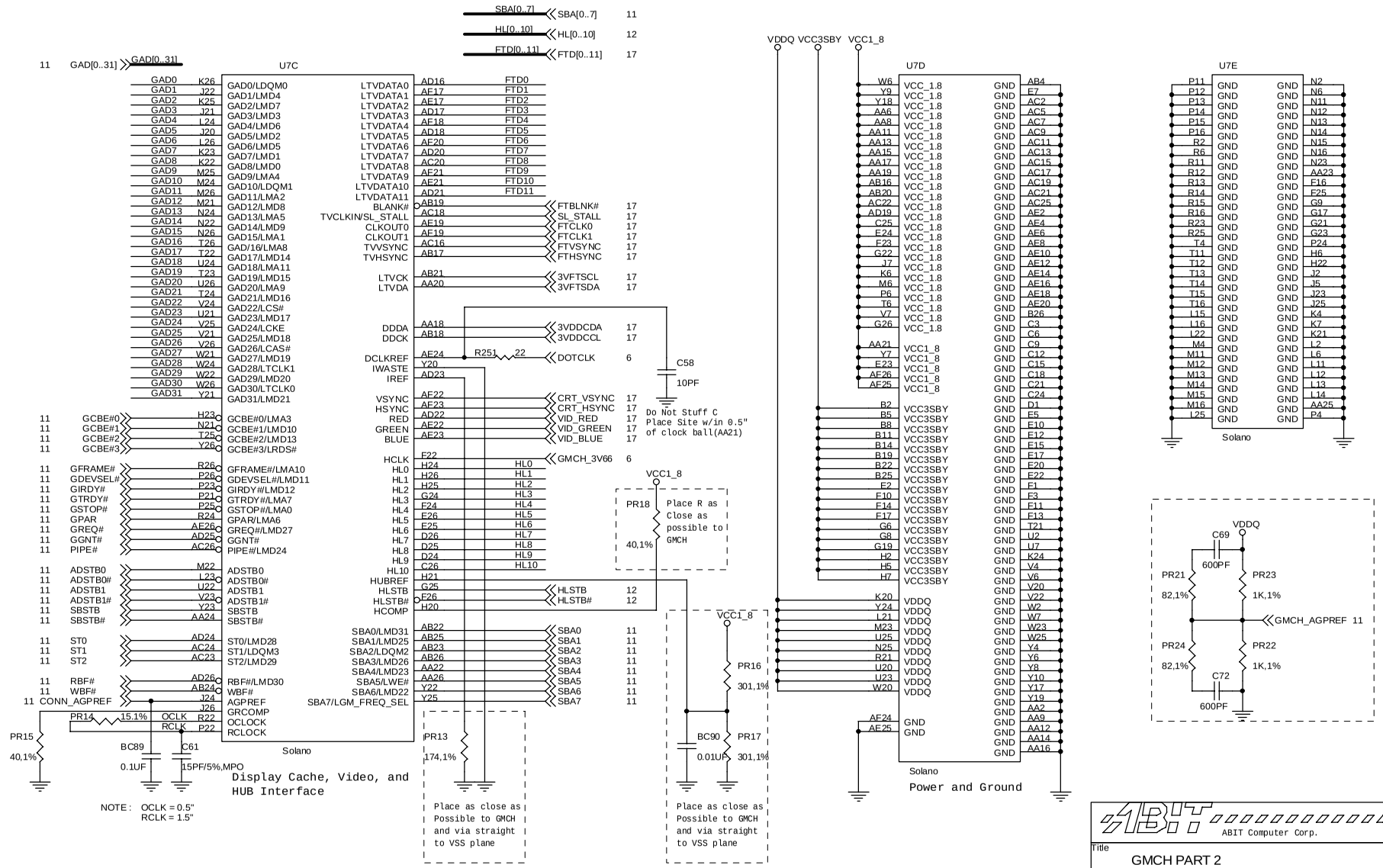
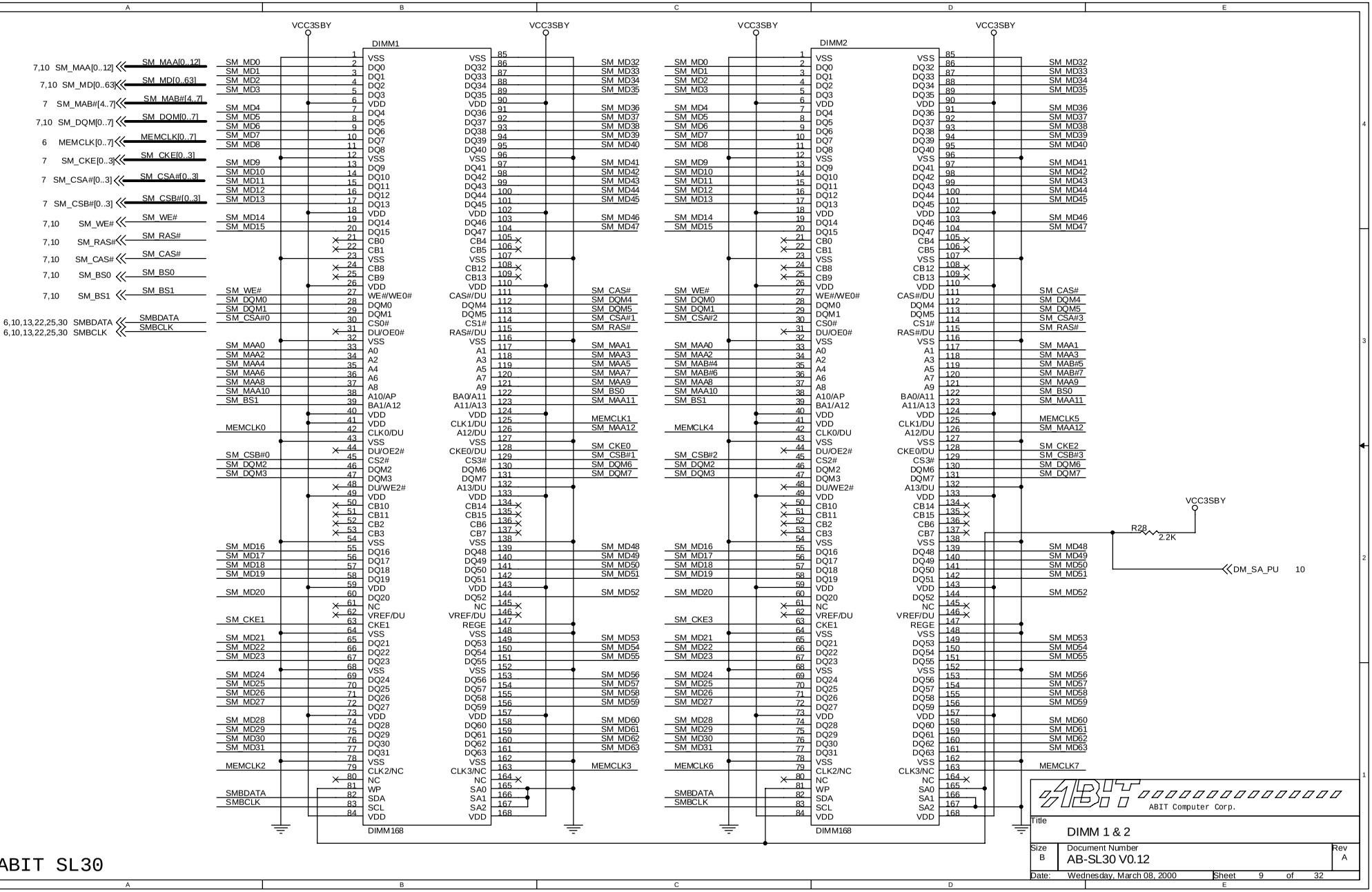
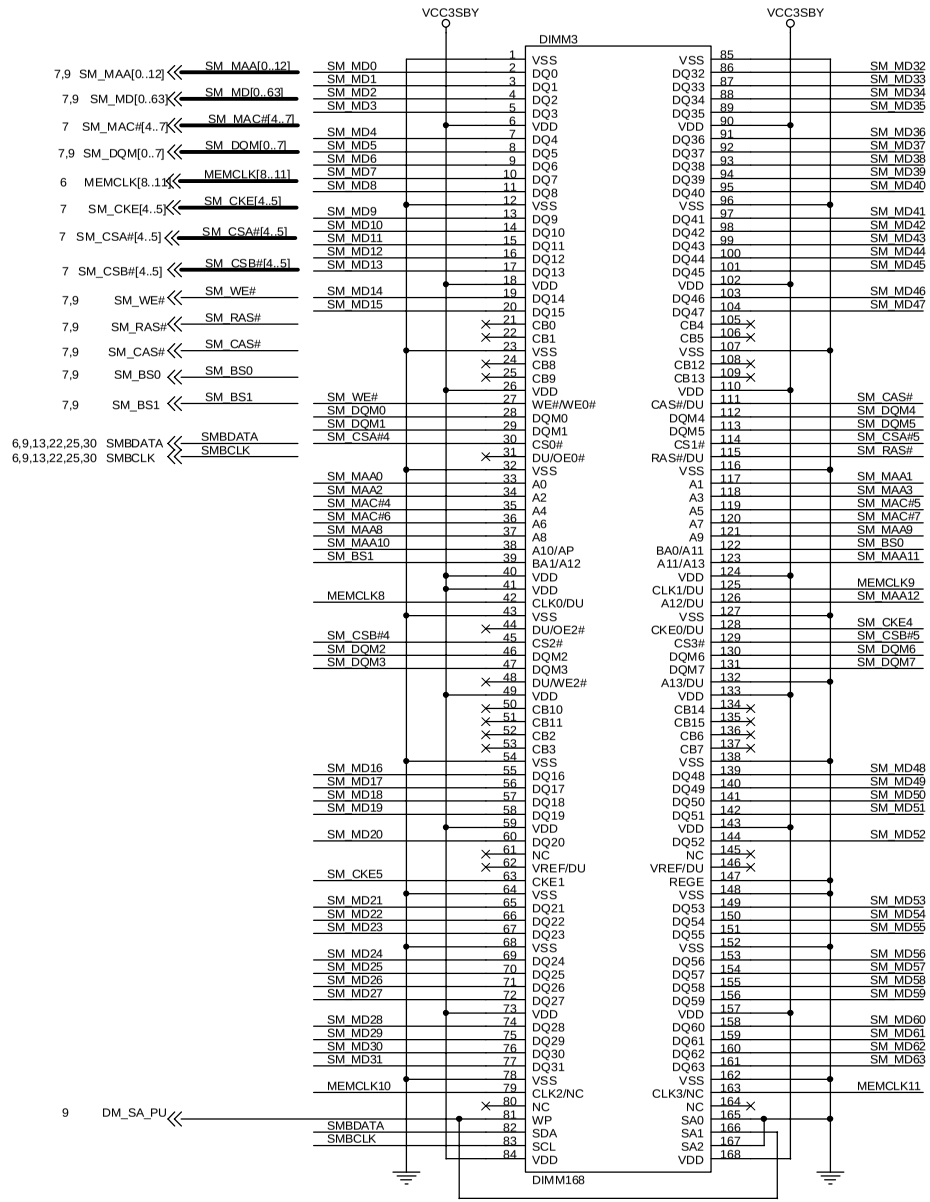
BPRI#
DBSY#
DRDY#
HIT#
HITM#
HTRDY#
3,5 HA#[3..31]
HA#[3..31]
HA#0 HA#1 HA#2 HA#3 HA#4 HA#5 HA#6 HA#7 HA#8 HA#9 HA#10 HA#11 HA#12 HA#13 HA#14 HA#15 HA#16 HA#17 HA#18 HA#19 HA#20 HA#21 HA#22 HA#23 HA#24 HA#25 HA#26 HA#27 HA#28 HA#29 HA#30 HA#31
3,5 HREQ#0 HREQ#1 HREQ#2 HREQ#3 HREQ#4
3,5 RS#0 3,5 RS#1 3,5 RS#2
RS#0 RS#1 RS#2
Do Not Stuff C
Place Site w/in
0.5" of clock
ball(v6)
C38
X18PF
Host Interface
HD#[0..63]
3,5
HD#0 HD#1 HD#2 HD#3 HD#4 HD#5 HD#6 HD#7 HD#8 HD#9 HD#10 HD#11 HD#12 HD#13 HD#14 HD#15 HD#16 HD#17 HD#18 HD#19 HD#20 HD#21 HD#22 HD#23 HD#24 HD#25 HD#26 HD#27 HD#28 HD#29 HD#30 HD#31 HD#32 HD#33 HD#34 HD#35 HD#36 HD#37 HD#38 HD#39 HD#40 HD#41 HD#42 HD#43 HD#44 HD#45 HD#46 HD#47 HD#48 HD#49 HD#50 HD#51 HD#52 HD#53 HD#54 HD#55 HD#56 HD#57 HD#58 HD#59 HD#60 HD#61 HD#62 HD#63
10 SM_MAC#[4..7]
9 SM_MAB#[4..7]
9,10 SM_MAA[0..12]
SM_MAC#[4..7]
SM_MAB#[4..7]
SM_MAA[0..12]
U7B
RN37
RN38 10/8P4R
10/8P4R
RN36 10/8P4R
9,10 SM_BS0
9,10 SM_BS1
9,10 SM_RAS#
9,10 SM_CAS#
9,10 SM_WE#
6 DCLK_WR
9,10 SM_DQM[0..7]
VCC3SBY
PR9 40,1%
C36
22PF
Solano
SYSTEM MEMORY
SM_MD[0..63]
SM_MD[0..63] 9,10
SMAA0 SMAA1 SMAA2 SMAA3 SMAA4 SMAA5 SMAA6 SMAA7 SMAA8 SMAA9 SMAA10 SMAA11 SMAA12
SMAB#4 SMAB#5 SMAB#6 SMAB#7
SMAC4 SMAC5 SMAC6 SMAC7
SBS0 SBS1
SCSA#0 SCSA#1 SCSA#2 SCSA#3 SCSA#4 SCSA#5
SCSB#0 SCSB#1 SCSB#2 SCSB#3 SCSB#4 SCSB#5
SRAS# SCAS# SWE#
SCKE0 SCKE1 SCKE2 SCKE3 SCKE4 SCKE5
SCLK RESVD
SDQM0 SDQM1 SDQM2 SDQM3 SDQM4 SDQM5 SDQM6 SDQM7
SRCOMP
SMD0 SMD1 SMD2 SMD3 SMD4 SMD5 SMD6 SMD7 SMD8 SMD9 SMD10 SMD11 SMD12 SMD13 SMD14 SMD15 SMD16 SMD17 SMD18 SMD19 SMD20 SMD21 SMD22 SMD23 SMD24 SMD25 SMD26 SMD27 SMD28 SMD29 SMD30 SMD31 SMD32 SMD33 SMD34 SMD35 SMD36 SMD37 SMD38 SMD39 SMD40 SMD41 SMD42 SMD43 SMD44 SMD45 SMD46 SMD47 SMD48 SMD49 SMD50 SMD51 SMD52 SMD53 SMD54 SMD55 SMD56 SMD57 SMD58 SMD59 SMD60 SMD61 SMD62 SMD63
D23 SM_MD0 C23 SM_MD1 D22 SM_MD2 F21 SM_MD3 E21 SM_MD4 G20 SM_MD5 F20 SM_MD6 D20 SM_MD7 F19 SM_MD8 E19 SM_MD9 D19 SM_MD10 E18 SM_MD11 B18 SM_MD12 F18 SM_MD13 G18 SM_MD14 D17 SM_MD15 A3 SM_MD16 A1 SM_MD17 C1 SM_MD18 F2 SM_MD19 G3 SM_MD20 D6 SM_MD21 C5 SM_MD22 B4 SM_MD23 D4 SM_MD24 C2 SM_MD25 D3 SM_MD26 E4 SM_MD27 F5 SM_MD28 G4 SM_MD29 J6 SM_MD30 K5 SM_MD31 A26 SM_MD32 A25 SM_MD33 B24 SM_MD34 A24 SM_MD35 B23 SM_MD36 A23 SM_MD37 C22 SM_MD38 A22 SM_MD39 D21 SM_MD40 B21 SM_MD41 A21 SM_MD42 C20 SM_MD43 B20 SM_MD44 A20 SM_MD45 C19 SM_MD46 A19 SM_MD47 A4 SM_MD48 A2 SM_MD49 B1 SM_MD50 E1 SM_MD51 G2 SM_MD52 E6 SM_MD53 D5 SM_MD54 C4 SM_MD55 B3 SM_MD56 D2 SM_MD57 E3 SM_MD58 F4 SM_MD59 F6 SM_MD60 G5 SM_MD61 H4 SM_MD62 J4 SM_MD63
VCC3SBY
BC188 BC190 BC191 BC189
X0.1UF X0.1UF X0.1UF X0.1UF
Backside decouping , should be placed under chipset memory signal field
VDDQ
BC192 BC193 BC194 BC195
X0.1UF X0.1UF X0.1UF X0.1UF
Backside decouping , should be placed under chipset AGP signal field
SM_WE# R90 8.2K R_BSEL#0 29
SM_CAS# R89 8.2K R_REFCLK 29
SM_MAA9 R88 8.2K VCOREDET 4
R68 X10K SM_MAA10
R77 X10K SM_RAS#
9 SM_CKE[0..3]
10 SM_CKE[4..5]
9 SM_CSA#[0..3]
10 SM_CSA#[4..5]
9 SM_CSB#[0..3]
10 SM_CSB#[4..5]
SM_CKE[0..3]
SM_CKE[4..5]
SM_CSA#[0..3]
SM_CSA#[4..5]
SM_CSB#[0..3]
SM_CSB#[4..5]
SM_WE# Host Freq : HI=100 LO=66
SM_MAA9 FSB P-MOS Kicker : HI=NON-Cu LO=Cu
SM_CAS# Host Freq : HI=133 LO=100/66
SBA7 LM FREQ : HI=133 LO=100
SM_BS0
SM_BS1 SM/LM muxing strap , active low
SM_MAA10 ALLZ : LO=ALLZ HI=Normal
SM_MAA11 IOQ depth : HI=4 LO=1
SM_MAA12 Slot vs. Socket : HI=Socket LO=SC242
SM_RAS# XOR chain : LO=XOR HI=Normal
ABIT Computer Corp.
Title
GMCH PART 1
Size B
Document Number
AB-SL30 V0.12
Rev A
Date: Wednesday, March 08, 2000
Sheet 7 of 32
ABIT SL30


U7C
U7D
U7E
Solano
Display Cache, Video, and HUB Interface
Power and Ground
NOTE : OCLK = 0.5"
RCLK = 1.5"
Do Not Stuff C
Place Site w/in 0.5" of clock ball(AA21)
Place R as Close as possible to GMCH
Place as close as Possible to GMCH and via straight to VSS plane
Place as close as Possible to GMCH and via straight to VSS plane
VDDQ
VCC3SBY
VCC1_8
GMCH_AGPREF
ABIT Computer Corp.
Title
GMCH PART 2
Size B
Document Number
AB-SL30 V0.12
Rev A
Date: Wednesday, March 08, 2000
Sheet 8 of 32

ABIT SL30


7,10 SM_MAA[0..12]
7,10 SM_MD[0..63]
7 SM_MAB#[4..7]
7,10 SM_DQM[0..7]
6 MEMCLK[0..7]
7 SM_CKE[0..3]
7 SM_CSA#[0..3]
7 SM_CSB#[0..3]
7,10 SM_WE#
7,10 SM_RAS#
7,10 SM_CAS#
7,10 SM_BS0
7,10 SM_BS1
6,10,13,22,25,30 SMBDATA
6,10,13,22,25,30 SMBCLK
VCC3SBY
DIMM1
DIMM168
DIMM2
R28
2.2K
DM_SA_PU 10
ABIT Computer Corp.
Title
DIMM 1 & 2
Size B
Document Number AB-SL30 V0.12
Rev A
Date: Wednesday, March 08, 2000
Sheet 9 of 32
ABIT SL30


VCC3SBY
VCC3SBY
DIMM3
DIMM168
SM_MAA[0..12]
SM_MD[0..63]
SM_MAC#[4..7]
SM_DQM[0..7]
MEMCLK[8..11]
SM_CKE[4..5]
SM_CSA#[4..5]
SM_CSB#[4..5]
SM_WE#
SM_RAS#
SM_CAS#
SM_BS0
SM_BS1
SMBDATA
SMBCLK
DM_SA_PU
VSS DQ0 DQ1 DQ2 DQ3 VDD DQ4 DQ5 DQ6 DQ7 VDD DQ8 VSS DQ9 DQ10 DQ11 DQ12 DQ13 VDD DQ14 DQ15 CB0 CB1 VSS CB8 CB9 VDD WE#/WE0# DQM0 DQM1 CS0# DU/OE0# VSS A0 A2 A4 A6 A8 A10/AP BA1/A12 VDD VDD CLK0/DU VSS DU/OE2# CS2# DQM2 DQM3 DU/WE2# VDD CB10 CB11 CB2 CB3 VSS DQ16 DQ17 DQ18 DQ19 VDD DQ20 NC VREF/DU CKE1 VSS DQ21 DQ22 DQ23 VSS DQ24 DQ25 DQ26 DQ27 VDD DQ28 DQ29 DQ30 DQ31 VSS CLK2/NC NC WP SDA SCL VDD
VSS DQ32 DQ33 DQ34 DQ35 VDD DQ36 DQ37 DQ38 DQ39 DQ40 VSS DQ41 DQ42 DQ43 DQ44 DQ45 VDD DQ46 DQ47 CB4 CB5 VSS CB12 CB13 VDD CAS#/DU DQM4 DQM5 CS1# RAS#/DU VSS A1 A3 A5 A7 A9 BA0/A11 A11/A13 VDD CLK1/DU A12/DU VSS CKE0/DU CS3# DQM6 DQM7 A13/DU VDD CB14 CB15 CB6 CB7 VSS DQ48 DQ49 DQ50 DQ51 VDD DQ52 NC VREF/DU REGE VSS DQ53 DQ54 DQ55 VSS DQ56 DQ57 DQ58 DQ59 VDD DQ60 DQ61 DQ62 DQ63 VSS CLK3/NC NC SA0 SA1 SA2 VDD

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ABIT Computer Corp.

Title: DIMM 3		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
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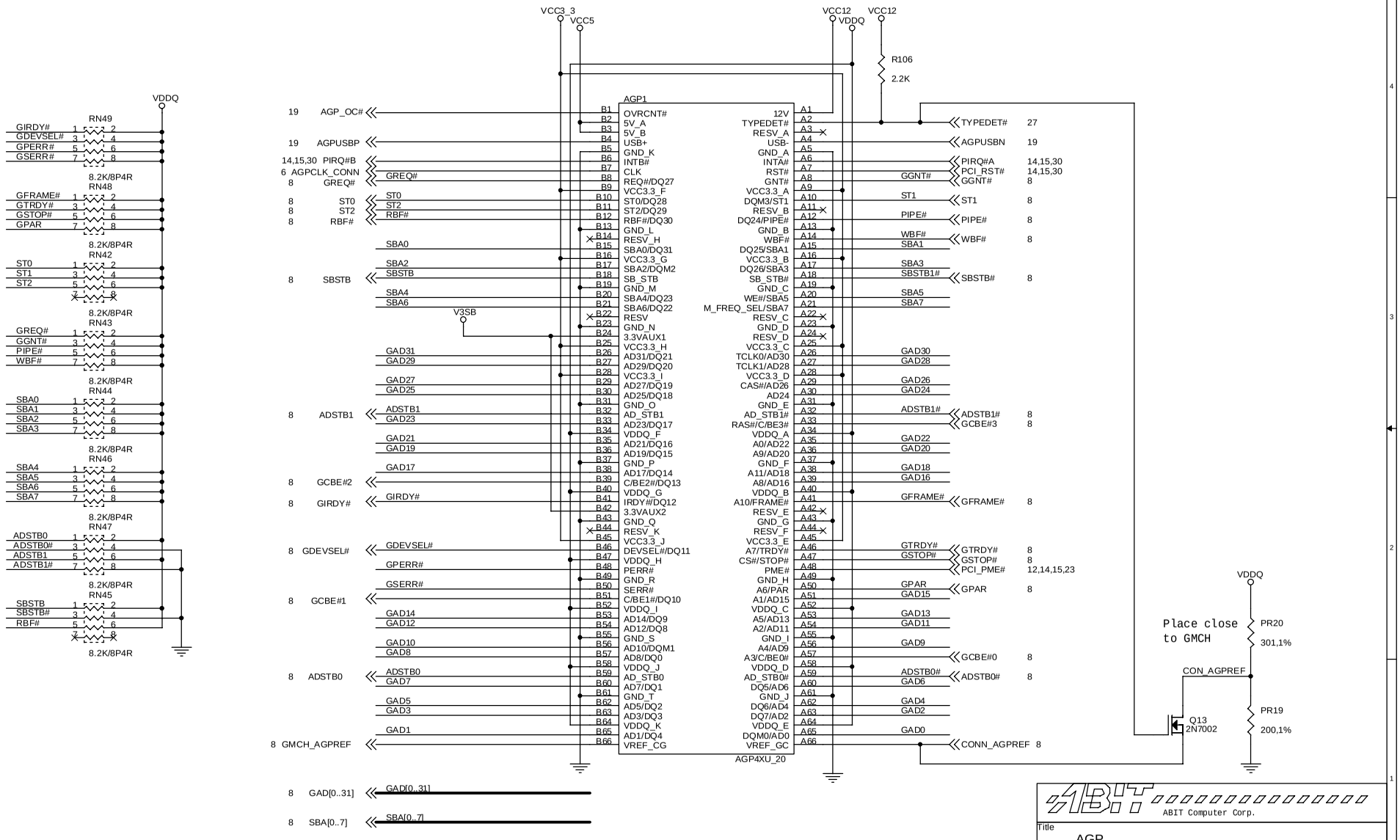
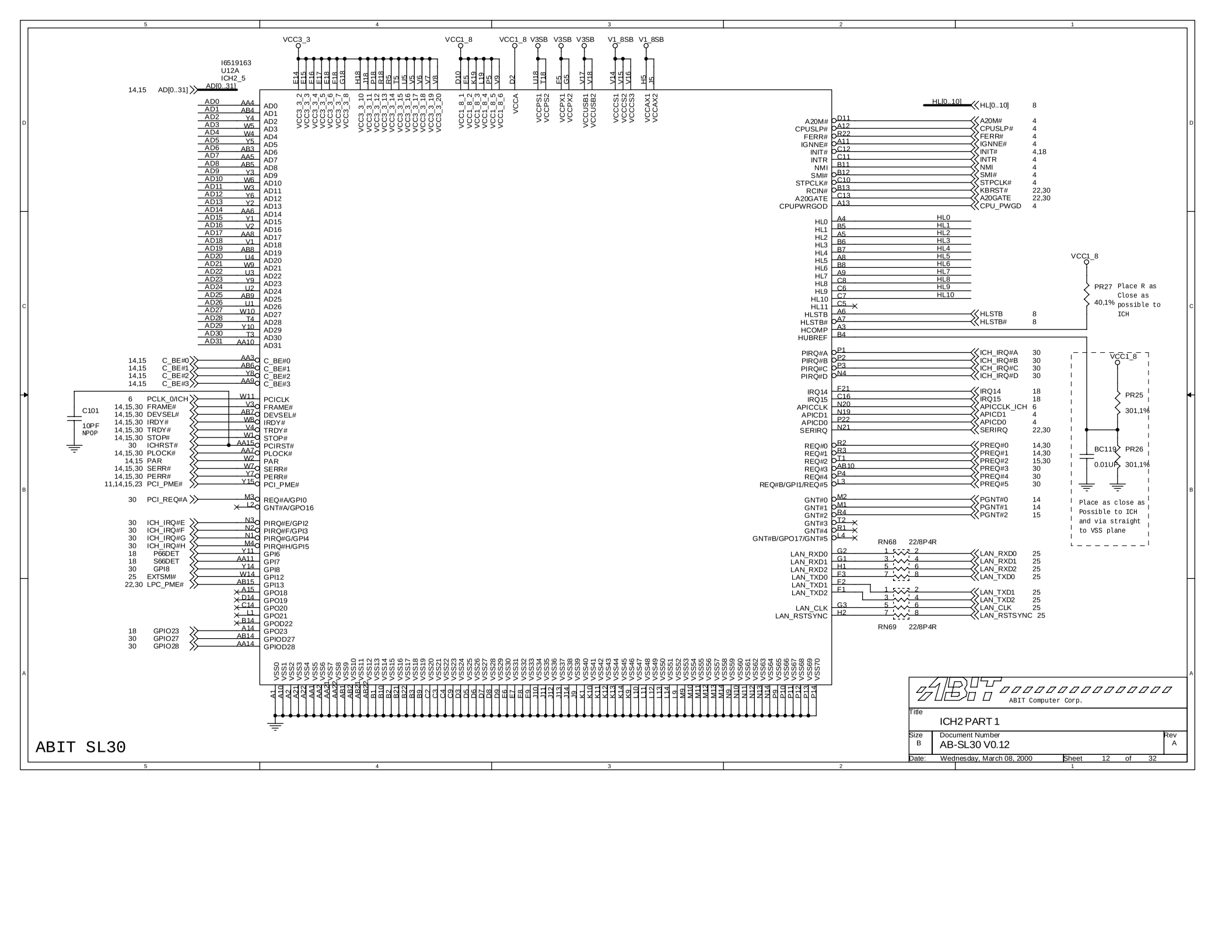
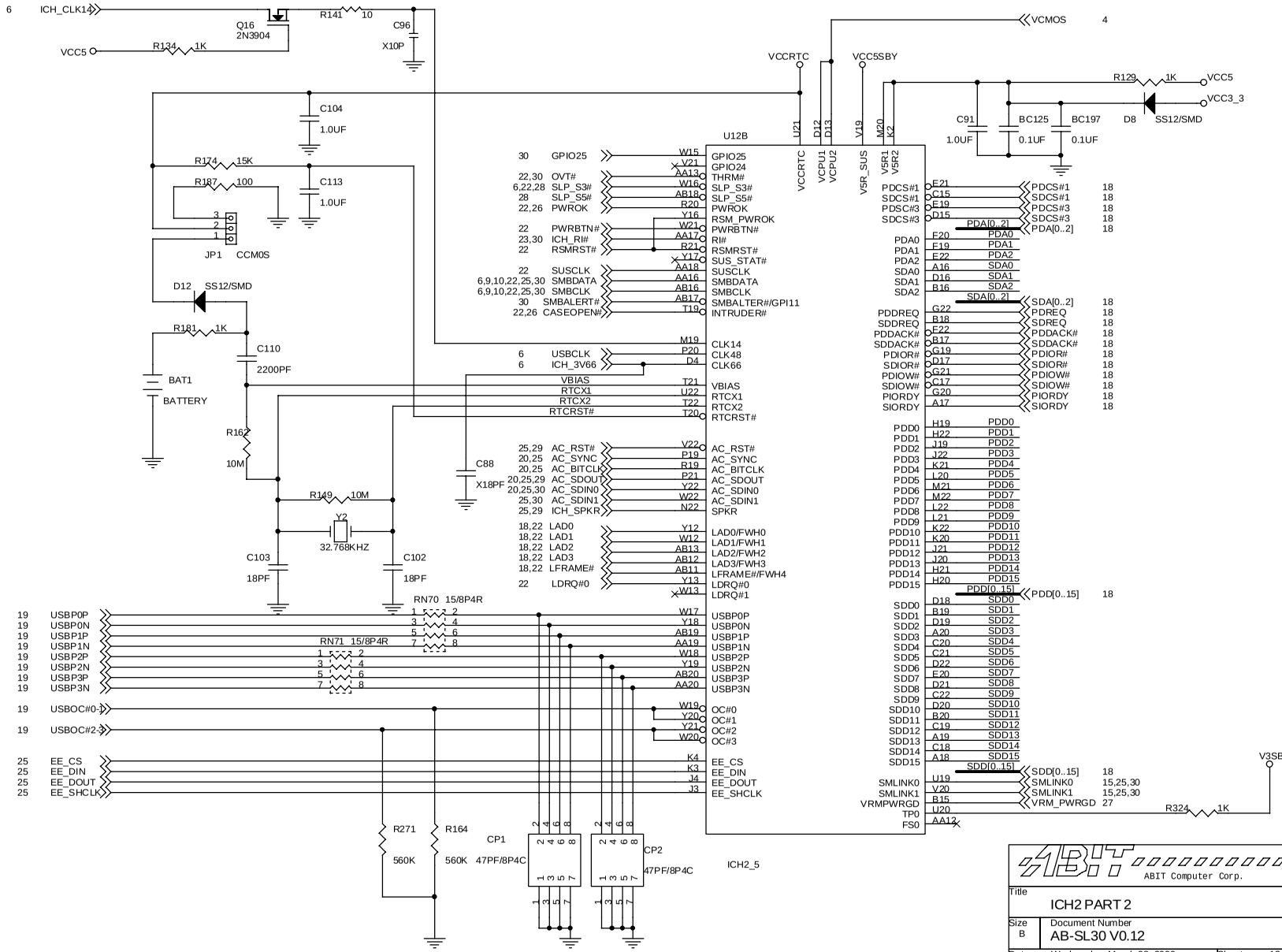


ABIT SL30

ABIT Computer Corp.

Title: AGP		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
Date: Wednesday, March 08, 2000	Sheet 11 of 32	

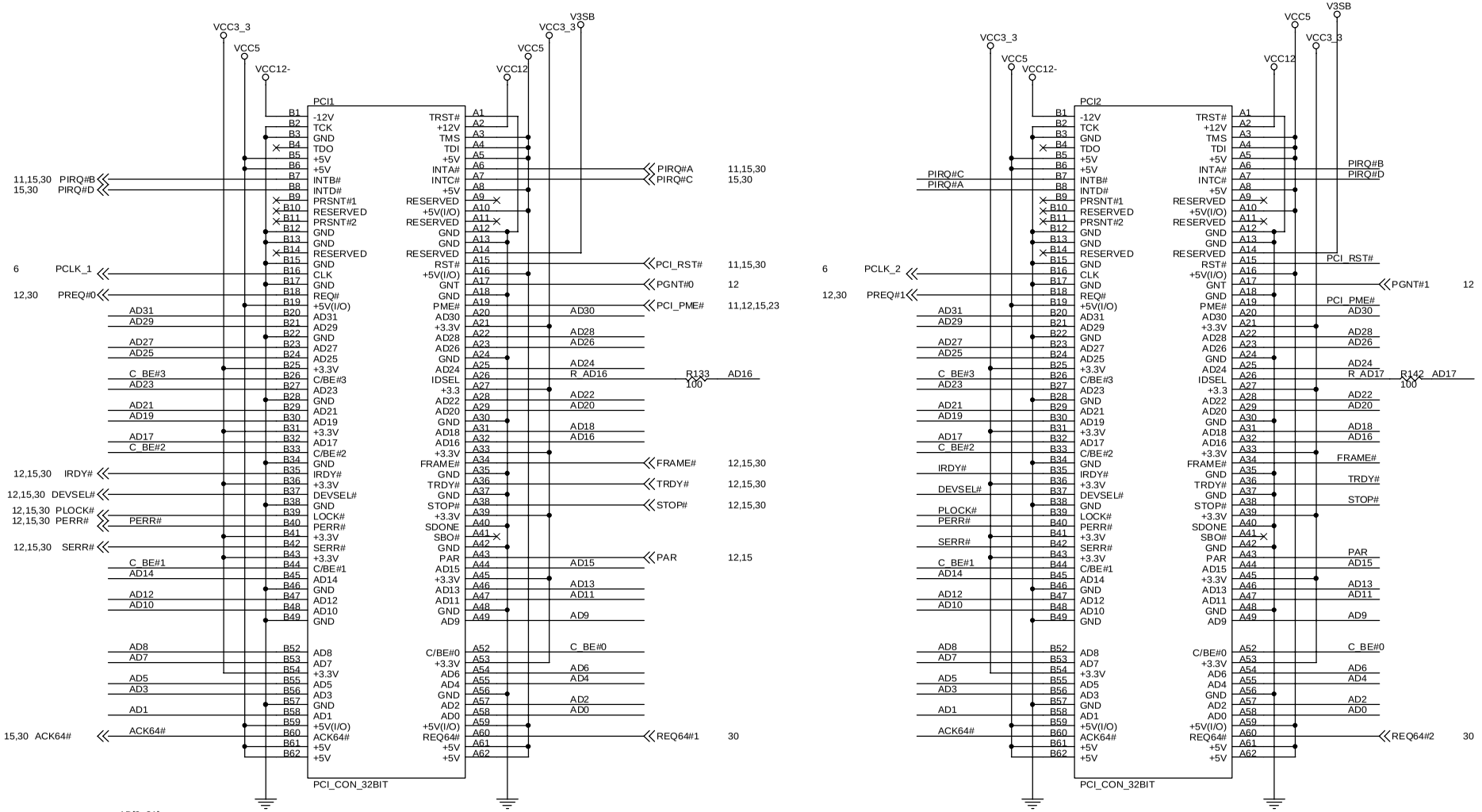

I6519163
U12A
ICH2_5
AD[0..31]
HL[0..10]
C101
10PF
NP0P
PR27
40,1%
Place R as Close as possible to ICH
PR25
301,1%
BC119
0.01UF
PR26
Place as close as Possible to ICH and via straight to VSS plane
RN68 22/8P4R
RN69 22/8P4R
ABIT SL30
ABIT Computer Corp.
Title
ICH2 PART 1
Size B
Document Number AB-SL30 V0.12
Rev A
Date: Wednesday, March 08, 2000
Sheet 12 of 32



ABIT SL30

ABIT Computer Corp.

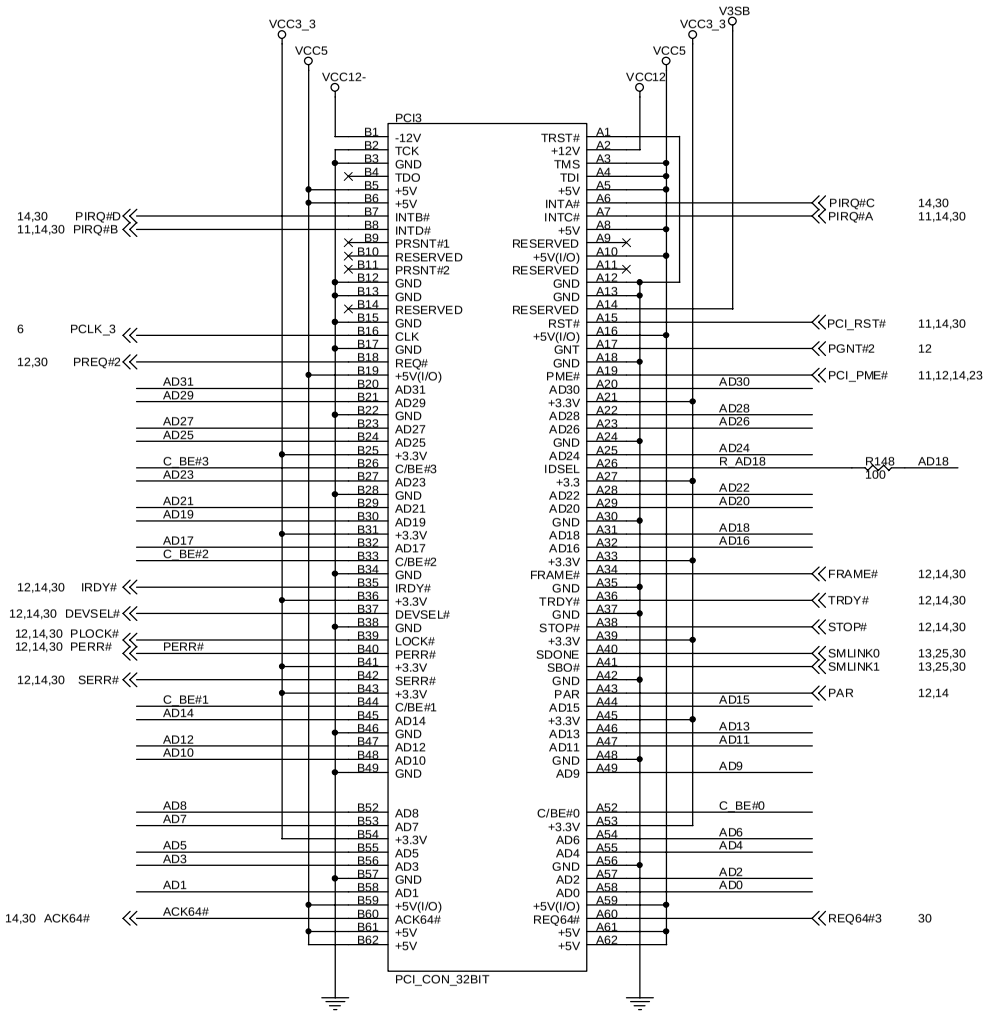
Title	ICH2 PART 2	
Size B	Document Number AB-SL30 V0.12	Rev A
Date: Wednesday, March 08, 2000	Sheet 13 of 32	



ABIT SL30

ABIT Computer Corp.

Title: PCI 1 & 2		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
Date: Wednesday, March 08, 2000	Sheet 14 of 32	



ABIT SL30

ABIT Computer Corp.

Title: PCI 3		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
Date: Wednesday, March 08, 2000	Sheet 15 of 32	

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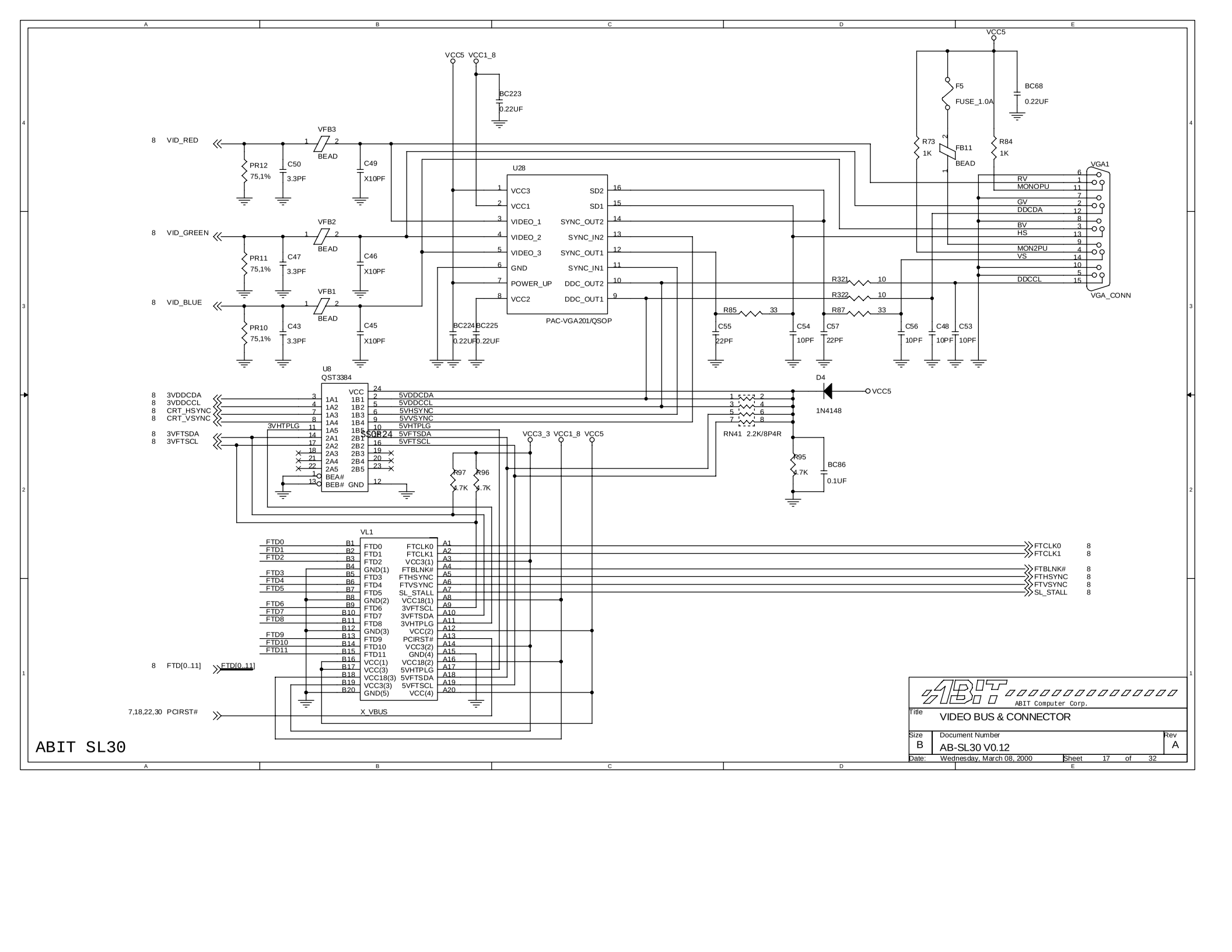
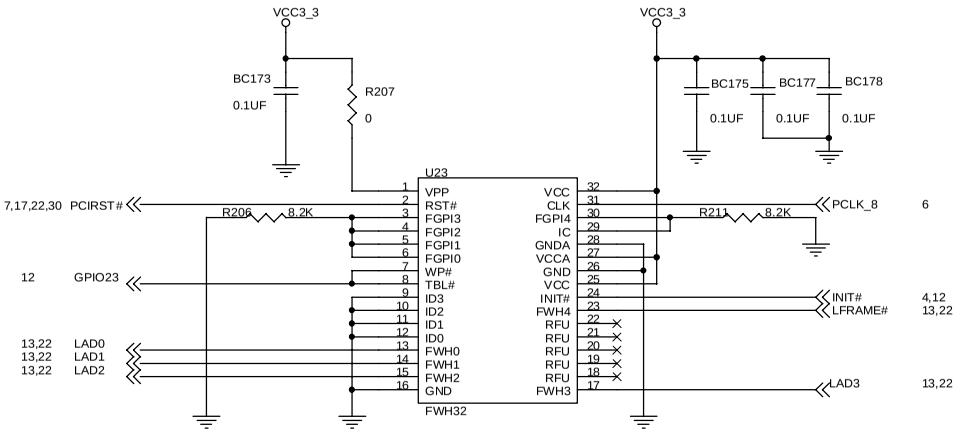
ABIT SL30

ABIT Computer Corp.

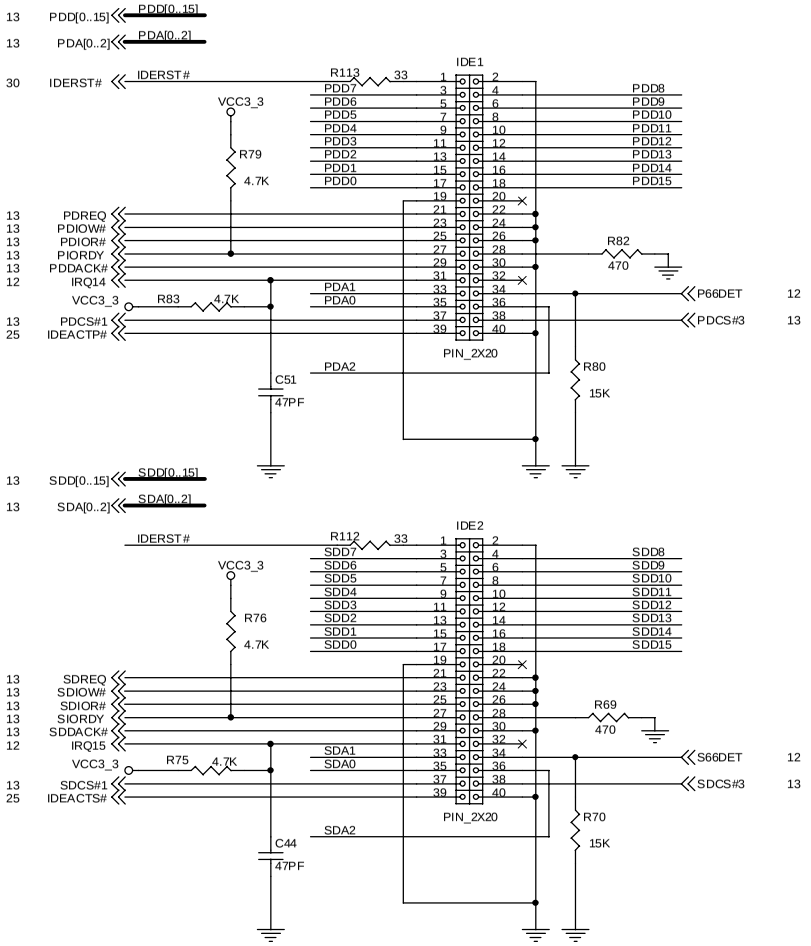
Title: LEFT BLANK		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
Date: Wednesday, March 08, 2000	Sheet 16 of 32	


VCC5
VCC5 VCC1_8
BC223
0.22UF
F5
FUSE_1.0A
BC68
0.22UF
R73
1K
FB11
BEAD
R84
1K
VGA1
VFB3
8 VID_RED
BEAD
PR12
75,1%
C50
3.3PF
C49
X10PF
U28
VFB2
8 VID_GREEN
BEAD
PR11
75,1%
C47
3.3PF
C46
X10PF
VCC3
VCC1
VIDEO_1
VIDEO_2
VIDEO_3
GND
POWER_UP
VCC2
SD2
SD1
SYNC_OUT2
SYNC_IN2
SYNC_OUT1
SYNC_IN1
DDC_OUT2
DDC_OUT1
PAC-VGA201/QSOP
RV
MONOPU
GV
DDCDA
BV
HS
MON2PU
VS
DDCCL
VGA_CONN
VFB1
8 VID_BLUE
BEAD
PR10
75,1%
C43
3.3PF
C45
X10PF
BC224
0.22UF
BC225
0.22UF
R321
10
R322
10
R85
33
R87
33
C55
22PF
C54
10PF
C57
22PF
C56
10PF
C48
10PF
C53
10PF
U8
QST3384
VCC
1A1
1A2
1A3
1A4
1A5
2A1
2A2
2A3
2A4
2A5
BEA#
BEB#
GND
1B1
1B2
1B3
1B4
1B5
2B1
2B2
2B3
2B4
2B5
8 3VDDCDA
8 3VDDCCL
8 CRT_HSYNC
8 CRT_VSYNC
8 3VFTSDA
8 3VFTSCL
3VHTPLG
5VDDCDA
5VDDCCL
5VHSYNC
5VVSYNC
5VHTPLG
5VFTSDA
5VFTSCL
D4
1N4148
VCC5
RN41 2.2K/8P4R
R95
4.7K
BC86
0.1UF
VCC3_3 VCC1_8 VCC5
R97
4.7K
R96
4.7K
VL1
FTD0
FTD1
FTD2
GND(1)
FTD3
FTD4
FTD5
GND(2)
FTD6
FTD7
FTD8
GND(3)
FTD9
FTD10
FTD11
VCC(1)
VCC(3)
VCC18(3)
VCC3(3)
GND(5)
FTCLK0
FTCLK1
VCC3(1)
FTBLNK#
FTHSYNC
FTVSYNC
SL_STALL
VCC18(1)
3VFTSCL
3VFTSDA
3VHTPLG
VCC(2)
PCIRST#
VCC3(2)
GND(4)
VCC18(2)
5VHTPLG
5VFTSCL
VCC(4)
FTCLK0 8
FTCLK1 8
FTBLNK# 8
FTHSYNC 8
FTVSYNC 8
SL_STALL 8
8 FTD[0..11]
FTD[0..11]
7,18,22,30 PCIRST#
X_VBUS
ABIT SL30
ABIT Computer Corp.
Title
VIDEO BUS & CONNECTOR
Size
B
Document Number
AB-SL30 V0.12
Rev
A
Date: Wednesday, March 08, 2000
Sheet 17 of 32

FWH



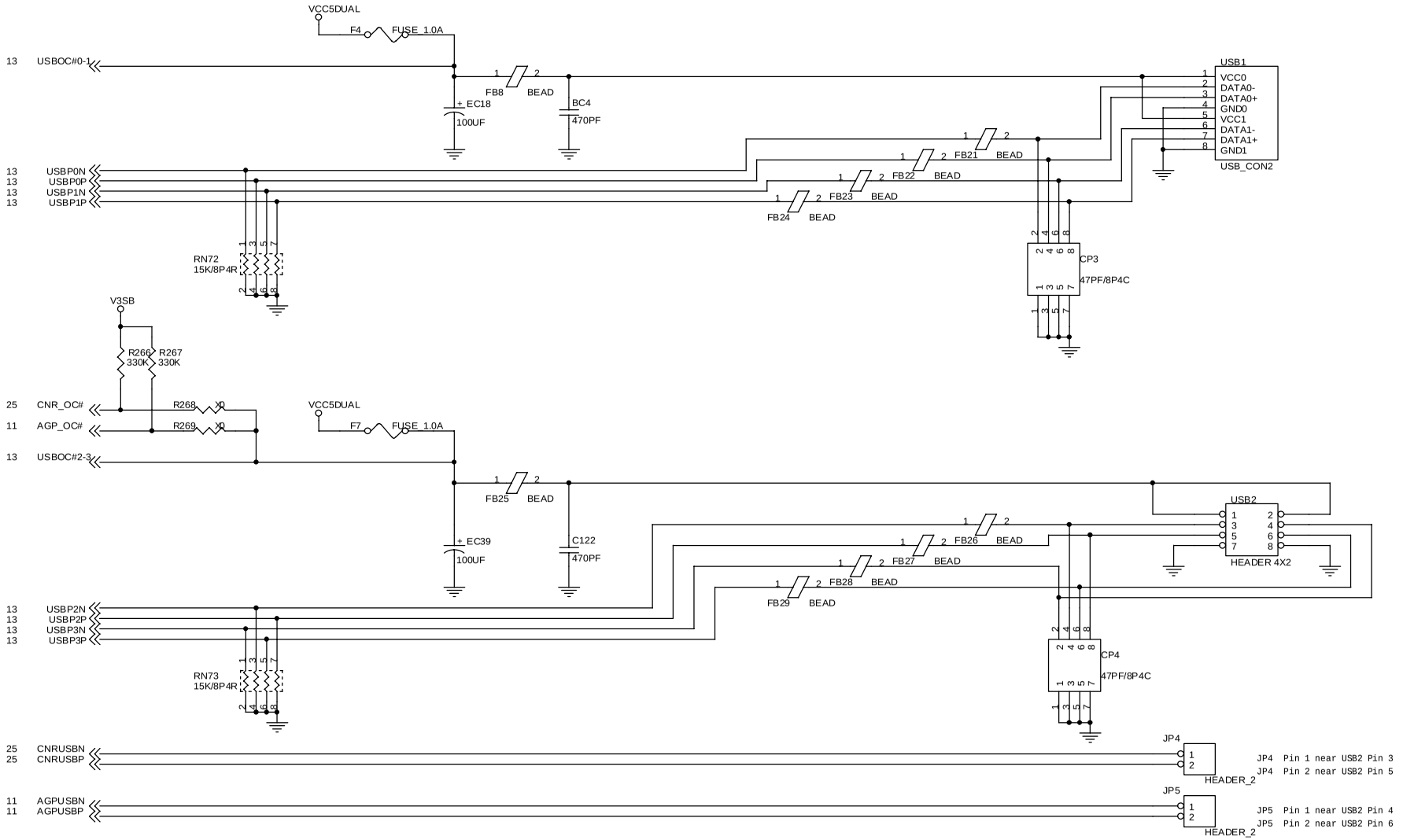
IDE



ABIT SL30

ABIT Computer Corp.

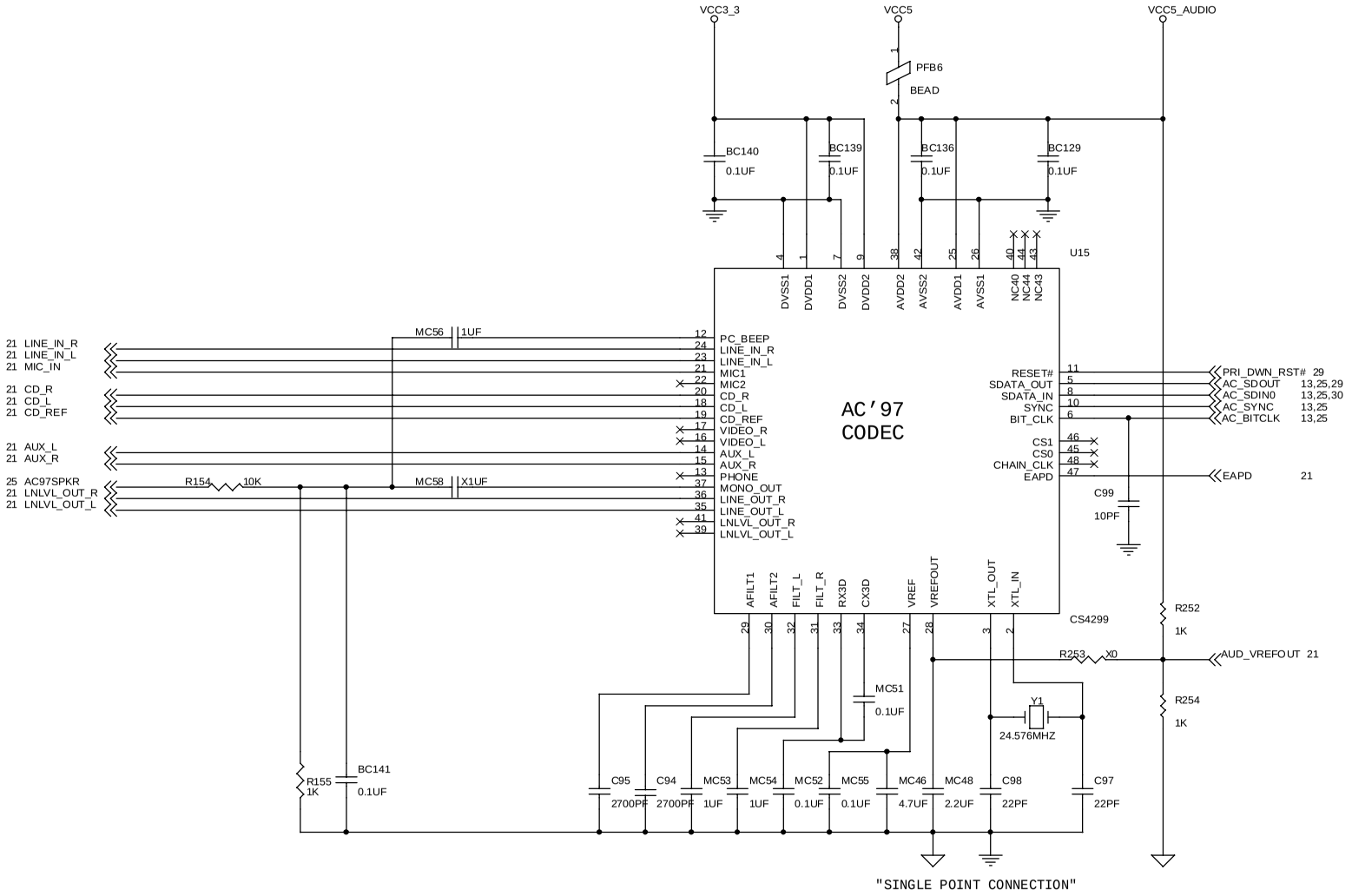
Title	FWH & UDAM100 IDE 1-2	
Size B	Document Number AB-SL30 V0.12	Rev A
Date: Wednesday, March 08, 2000	Sheet 18 of 32	



ABIT SL30

ABIT Computer Corp.

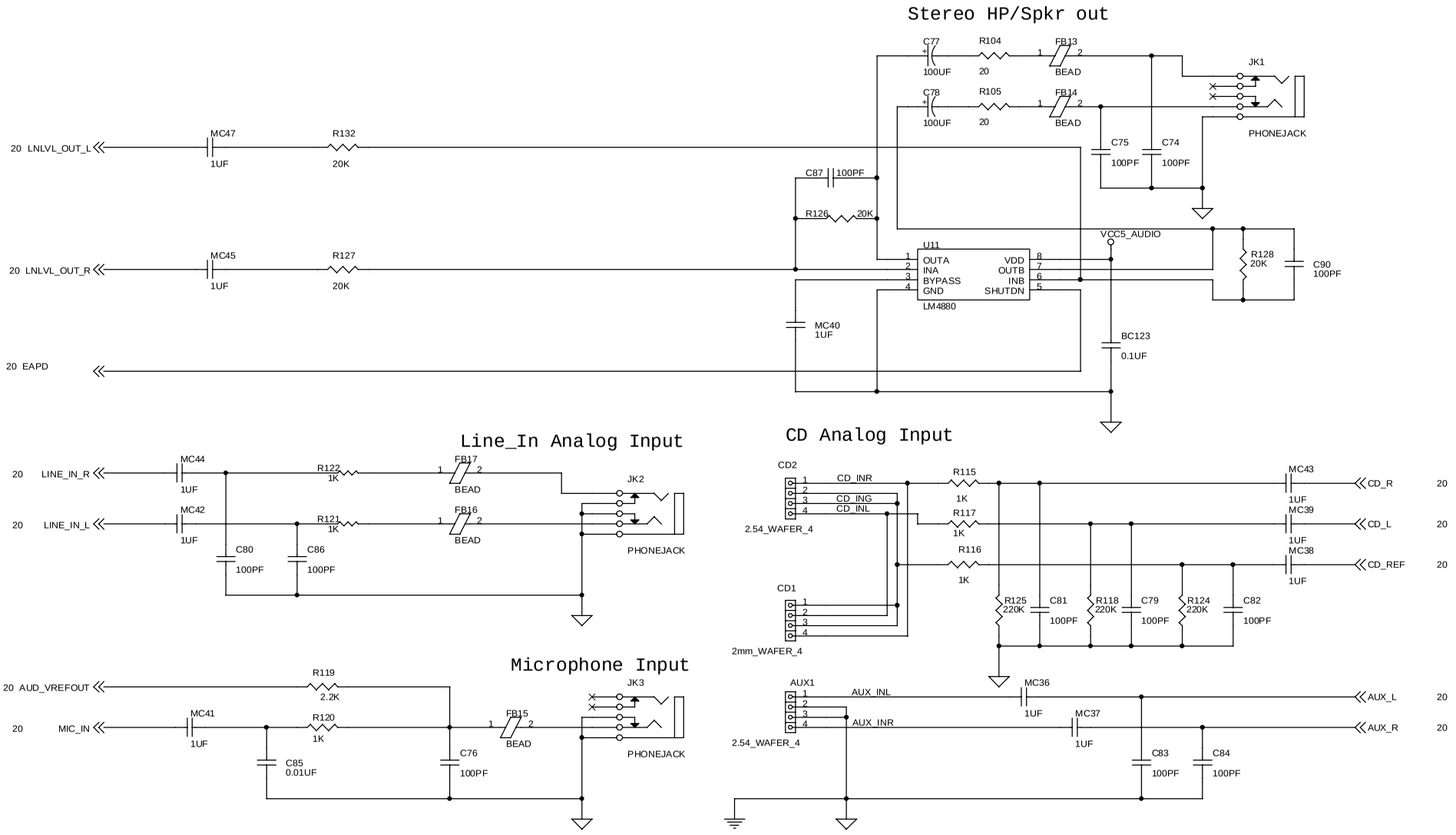
Title: USB 0-3		
Size: B	Document Number: AB-SL30 V0.12	Rev: A
Date: Wednesday, March 08, 2000	Sheet 19 of 32	



ABIT SL30

ABIT Computer Corp.

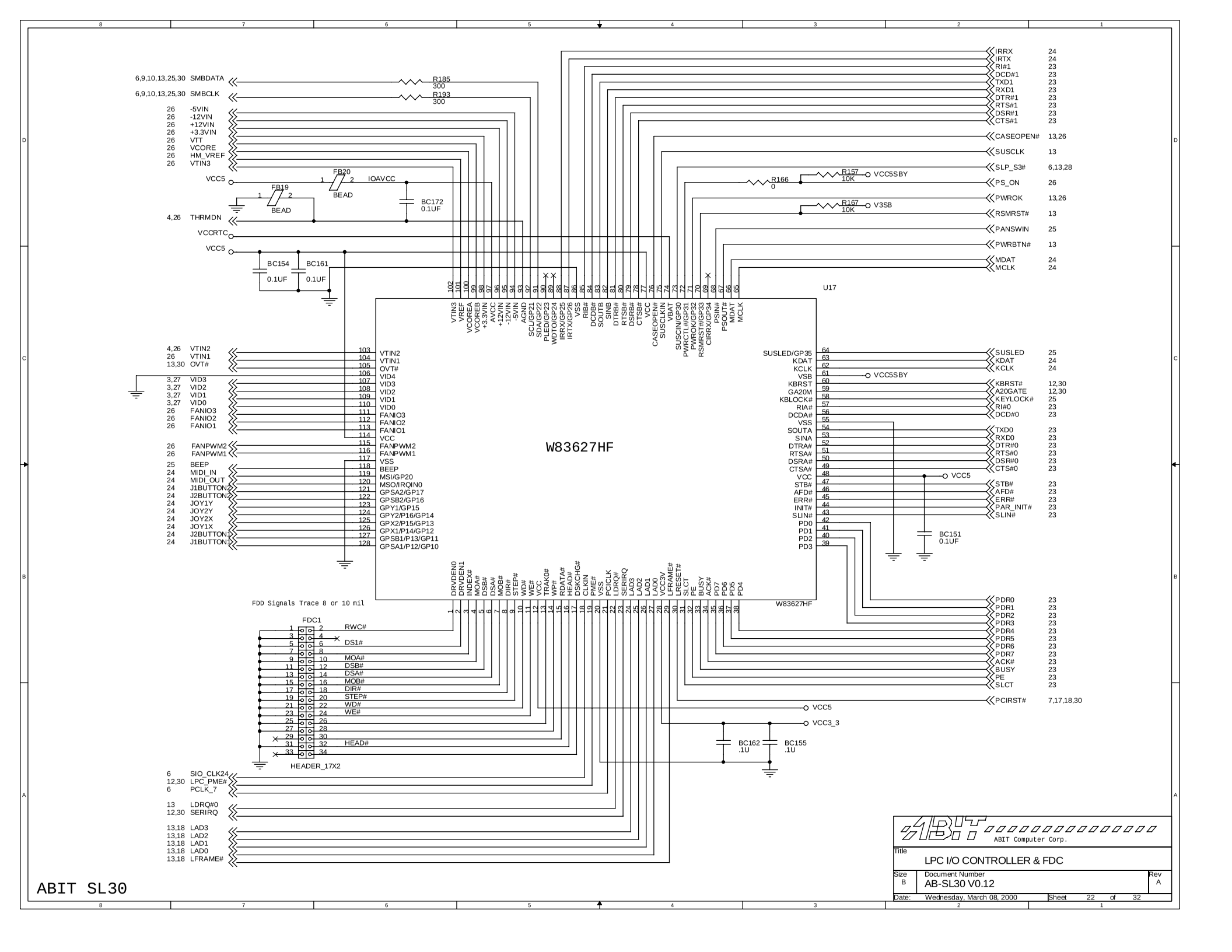
Title	AC97 CODEC	
Size B	Document Number AB-SL30 V0.12	Rev B
Date: Wednesday, March 08, 2000	Sheet 20 of 32	

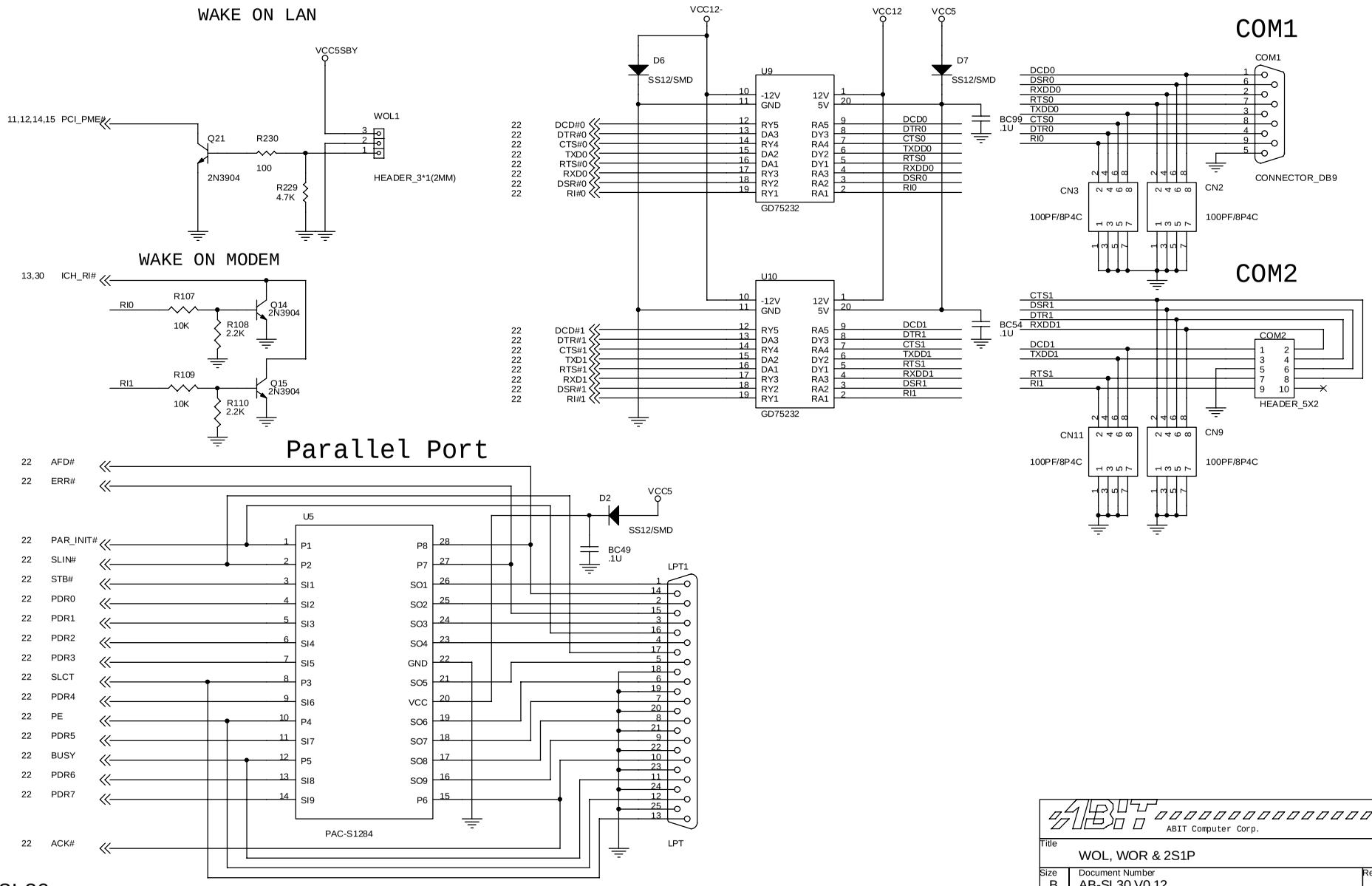


ABIT SL30

ABIT Computer Corp.

Title	AUDIO I/O	
Size B	Document Number AB-SL30 0.12	Rev A
Date: Wednesday, March 15, 2000	Sheet 21 of 32	


W83627HF
U17
FDD Signals Trace 8 or 10 mil
FDC1
HEADER_17X2
R185 300
R193 300
R157 10K
R166 0
R167 10K
BC172 0.1UF
BC154 0.1UF
BC161 0.1UF
BC151 0.1UF
BC162 .1U
BC155 .1U
FB19 BEAD
FB20 BEAD
IOAVCC
VCC5
VCC3_3
VCC5SBY
V3SB
ABIT SL30
ABIT Computer Corp.
LPC I/O CONTROLLER & FDC
AB-SL30 V0.12
Wednesday, March 08, 2000
Sheet 22 of 32


WAKE ON LAN
VCC5SBY
11,12,14,15 PCI_PME#
Q21
2N3904
R230
100
R229
4.7K
WOL1
HEADER_3*1(2MM)
WAKE ON MODEM
13,30 ICH_RI#
RI0
R107
10K
R108
2.2K
Q14
2N3904
RI1
R109
10K
R110
2.2K
Q15
2N3904
VCC12-
VCC12
VCC5
D6
SS12/SMD
D7
SS12/SMD
U9
-12V
GND
12V
5V
RY5
DA3
RY4
DA2
DA1
RY3
RY2
RY1
RA5
DY3
RA4
DY2
DY1
RA3
RA2
RA1
GD75232
DCD#0
DTR#0
CTS#0
TXD0
RTS#0
RXD0
DSR#0
RI#0
DCD0
DTR0
CTS0
TXDD0
RTS0
RXDD0
DSR0
RI0
BC99
.1U
U10
DCD#1
DTR#1
CTS#1
TXD1
RTS#1
RXD1
DSR#1
RI#1
DCD1
DTR1
CTS1
TXDD1
RTS1
RXDD1
DSR1
RI1
BC54
.1U
COM1
DCD0
DSR0
RXDD0
RTS0
TXDD0
CTS0
DTR0
RI0
CONNECTOR_DB9
CN3
CN2
100PF/8P4C
COM2
CTS1
DSR1
DTR1
RXDD1
DCD1
TXDD1
RTS1
RI1
HEADER_5X2
CN11
CN9
Parallel Port
AFD#
ERR#
PAR_INIT#
SLIN#
STB#
PDR0
PDR1
PDR2
PDR3
SLCT
PDR4
PE
PDR5
BUSY
PDR6
PDR7
ACK#
U5
P1
P2
SI1
SI2
SI3
SI4
SI5
P3
SI6
P4
SI7
P5
SI8
SI9
P8
P7
SO1
SO2
SO3
SO4
GND
SO5
VCC
SO6
SO7
SO8
SO9
P6
PAC-S1284
D2
SS12/SMD
BC49
.1U
LPT1
LPT
ABIT SL30
ABIT Computer Corp.
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WOL, WOR & 2S1P
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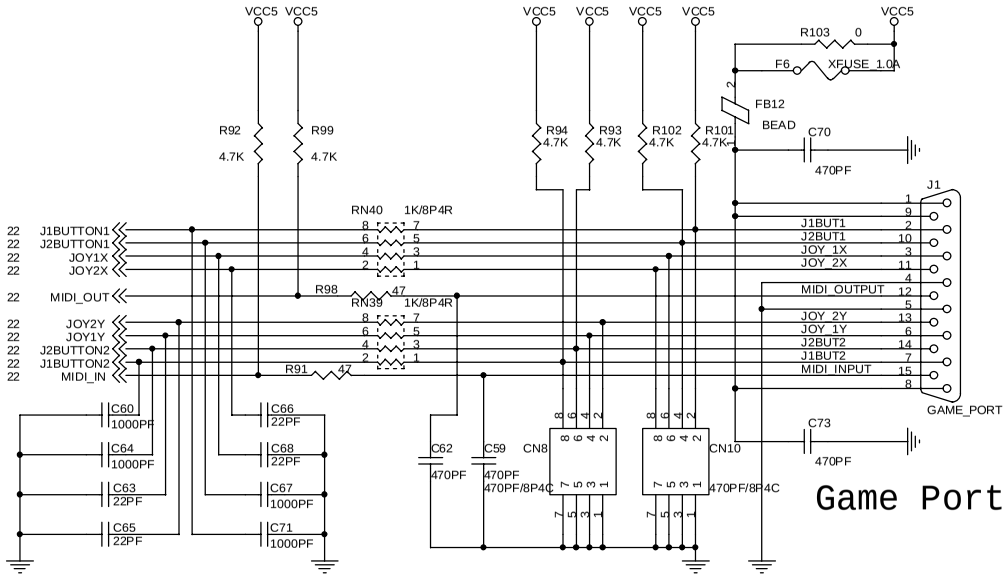

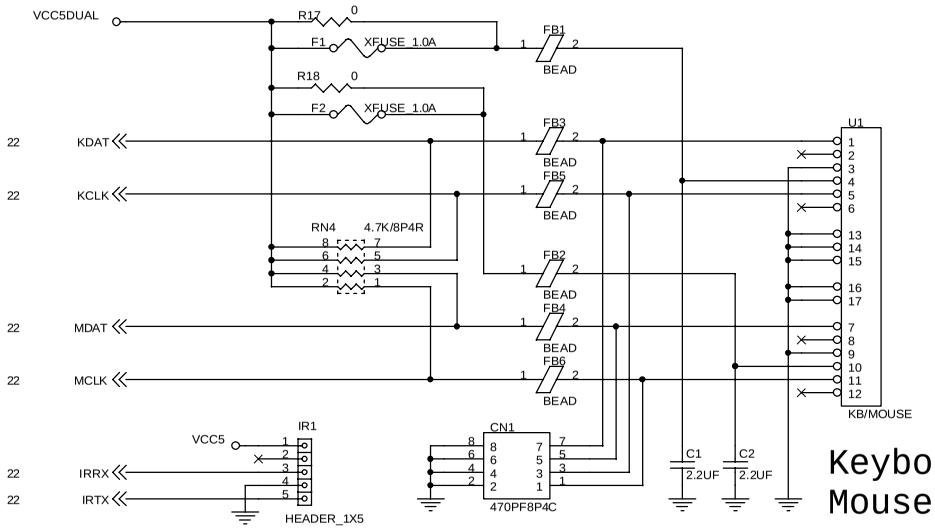

IR

ABIT SL30

ABIT Computer Corp.

Title: KB, MS, GAME ,WOL & IR		
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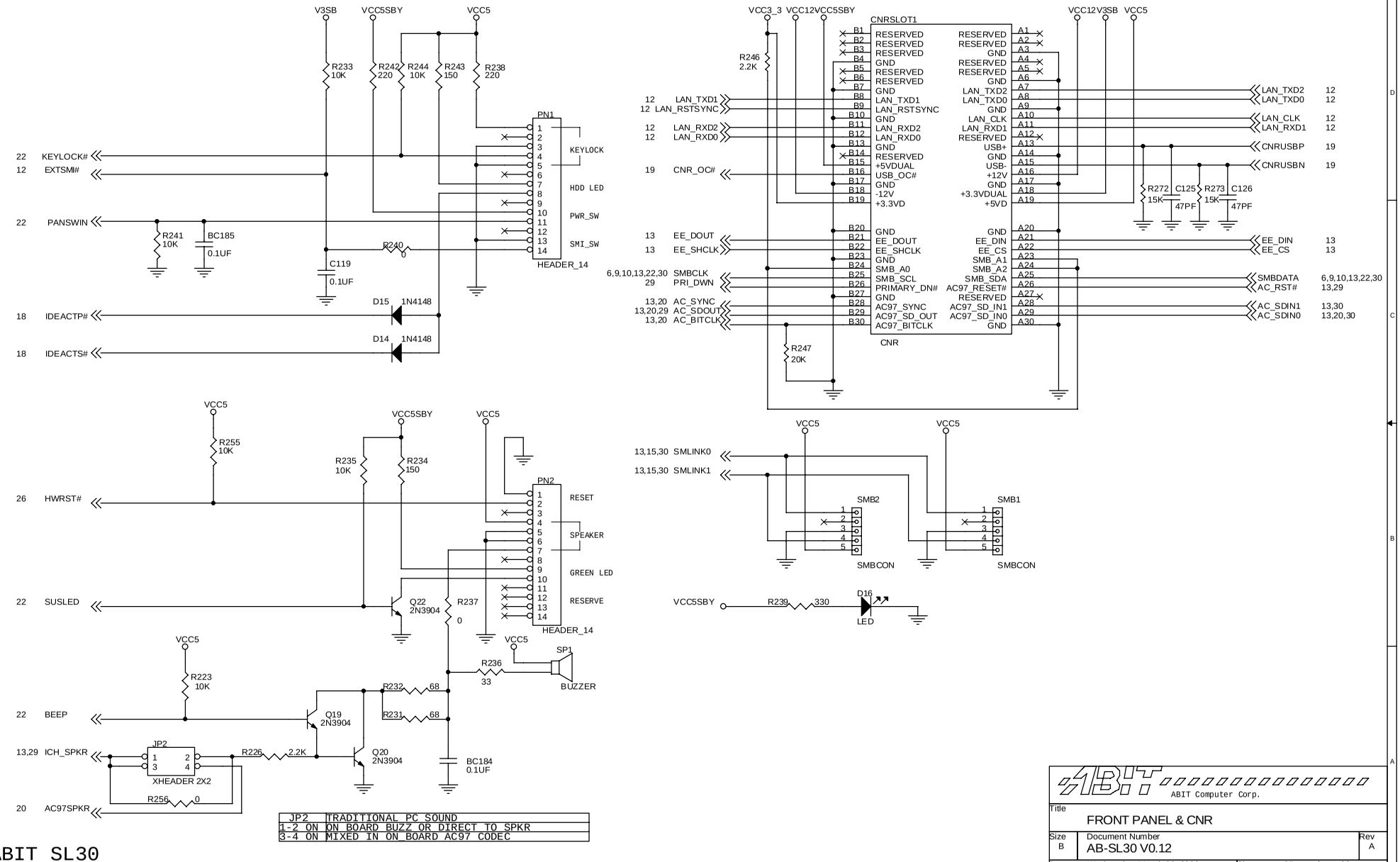
V3SB
VCC5SBY
VCC5
R233 10K
R242 220
R244 10K
R243 150
R238 220
PN1
KEYLOCK
HDD LED
PWR_SW
SMI_SW
HEADER_14
22 KEYLOCK#
12 EXTSMI#
22 PANSWIN
R241 10K
BC185 0.1UF
R240 0
C119 0.1UF
D15 1N4148
D14 1N4148
18 IDEACTP#
18 IDEACTS#
VCC3_3
VCC12
CNRSLOT1
RESERVED
GND
LAN_TXD1
LAN_RSTSYNC
LAN_RXD2
LAN_RXD0
+5VDUAL
USB_OC#
-12V
+3.3VD
LAN_TXD2
LAN_TXD0
LAN_CLK
LAN_RXD1
USB+
USB-
+12V
+3.3VDUAL
+5VD
AC97_SYNC
AC97_SD_OUT
AC97_BITCLK
AC97_SD_IN1
AC97_SD_IN0
AC97_RESET#
PRIMARY_DN#
CNR
R246 2.2K
R247 20K
12 LAN_TXD1
12 LAN_RSTSYNC
12 LAN_RXD2
12 LAN_RXD0
19 CNR_OC#
13 EE_DOUT
13 EE_SHCLK
6,9,10,13,22,30 SMBCLK
29 PRI_DWN
13,20 AC_SYNC
13,20,29 AC_SDOUT
13,20 AC_BITCLK
LAN_TXD2 12
LAN_TXD0 12
LAN_CLK 12
LAN_RXD1 12
CNRUSBP 19
CNRUSBN 19
R272 15K
C125 47PF
R273 15K
C126 47PF
EE_DIN 13
EE_CS 13
SMBDATA 6,9,10,13,22,30
AC_RST# 13,29
AC_SDIN1 13,30
AC_SDIN0 13,20,30
13,15,30 SMLINK0
13,15,30 SMLINK1
SMB2
SMB1
SMBCON
VCC5SBY
R239 330
D16
LED
R255 10K
R235 10K
R234 150
PN2
RESET
SPEAKER
GREEN LED
RESERVE
HEADER_14
26 HWRST#
22 SUSLED
Q22 2N3904
R237 0
R223 10K
R236 33
SP1
BUZZER
R232 68
R231 68
22 BEEP
Q19 2N3904
13,29 ICH_SPKR
JP2
XHEADER 2X2
R226 2.2K
Q20 2N3904
BC184 0.1UF
R256 0
20 AC97SPKR
JP2 TRADITIONAL PC SOUND
1-2 ON ON BOARD BUZZ OR DIRECT TO SPKR
3-4 ON MIXED IN ON BOARD AC97 CODEC
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ABIT Computer Corp.
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FRONT PANEL & CNR
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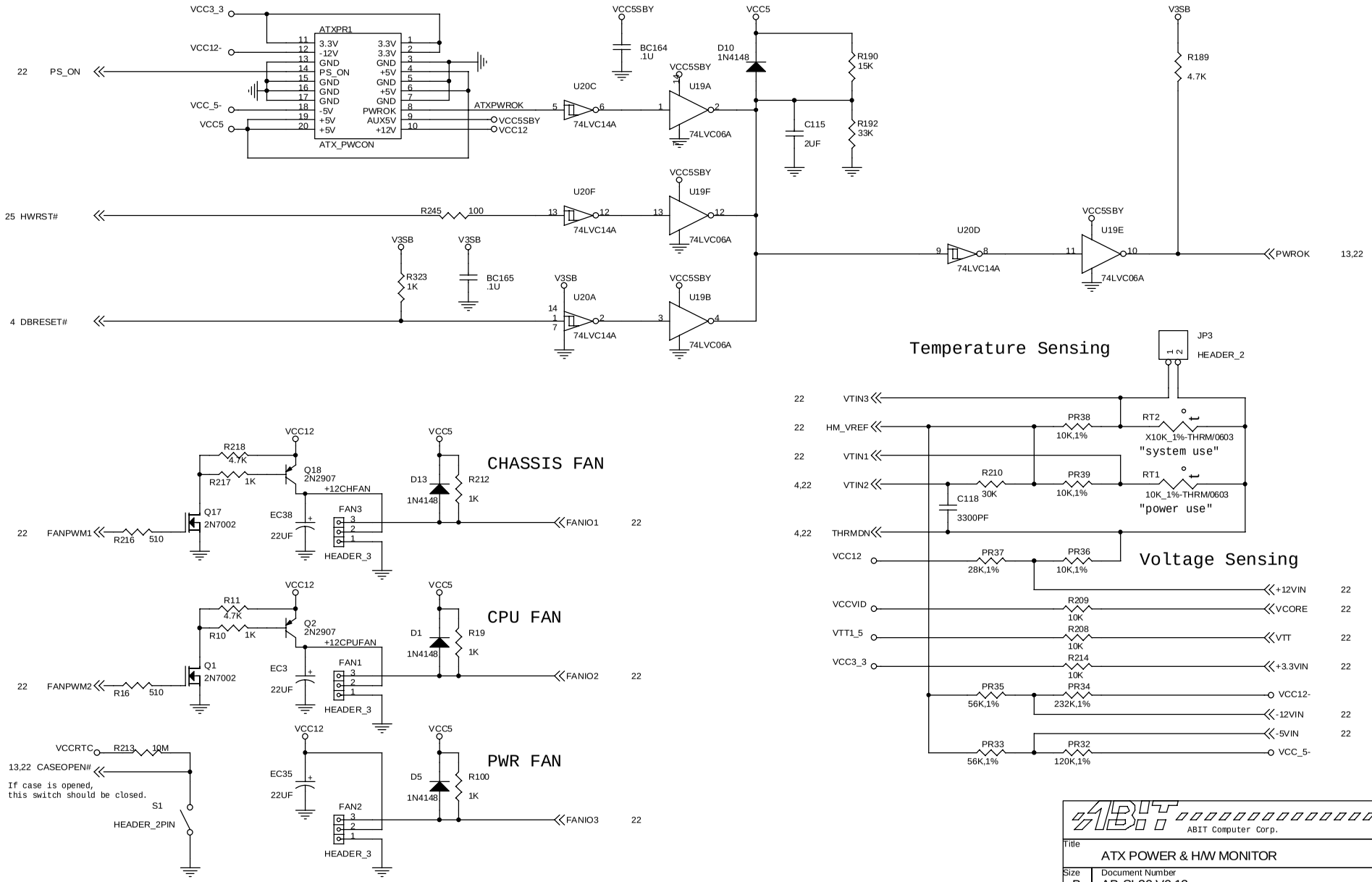
ATXPR1
ATX_PWCON
VCC3_3
VCC12-
VCC_5-
VCC5
22 PS_ON
ATXPWROK
VCC5SBY
VCC12
U20C
74LVC14A
U19A
74LVC06A
BC164
.1U
D10
1N4148
R190
15K
R192
33K
C115
2UF
V3SB
R189
4.7K
25 HWRST#
R245
100
U20F
U19F
4 DBRESET#
R323
1K
BC165
.1U
U20A
U19B
U20D
U19E
PWROK
13,22
Temperature Sensing
JP3
HEADER_2
22 VTIN3
22 HM_VREF
22 VTIN1
4,22 VTIN2
4,22 THRMDN
PR38
10K,1%
RT2
X10K_1%-THRM/0603
"system use"
R210
30K
PR39
10K,1%
RT1
10K_1%-THRM/0603
"power use"
C118
3300PF
Voltage Sensing
VCC12
PR37
28K,1%
PR36
10K,1%
+12VIN
VCCVID
R209
10K
VCORE
VTT1_5
R208
10K
VTT
VCC3_3
R214
10K
+3.3VIN
PR35
56K,1%
PR34
232K,1%
VCC12-
-12VIN
-5VIN
PR33
56K,1%
PR32
120K,1%
VCC_5-
CHASSIS FAN
R218
4.7K
R217
1K
Q18
2N2907
+12CHFAN
Q17
2N7002
22 FANPWM1
R216
510
EC38
22UF
FAN3
HEADER_3
D13
1N4148
R212
1K
FANIO1
CPU FAN
R11
4.7K
R10
1K
Q2
2N2907
+12CPUFAN
Q1
2N7002
22 FANPWM2
R16
510
EC3
22UF
FAN1
HEADER_3
D1
1N4148
R19
1K
FANIO2
PWR FAN
VCCRTC
R213
10M
13,22 CASEOPEN#
If case is opened,
this switch should be closed.
S1
HEADER_2PIN
EC35
22UF
FAN2
HEADER_3
D5
1N4148
R100
1K
FANIO3
ABIT SL30
ABIT Computer Corp.
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ATX POWER & H/W MONITOR
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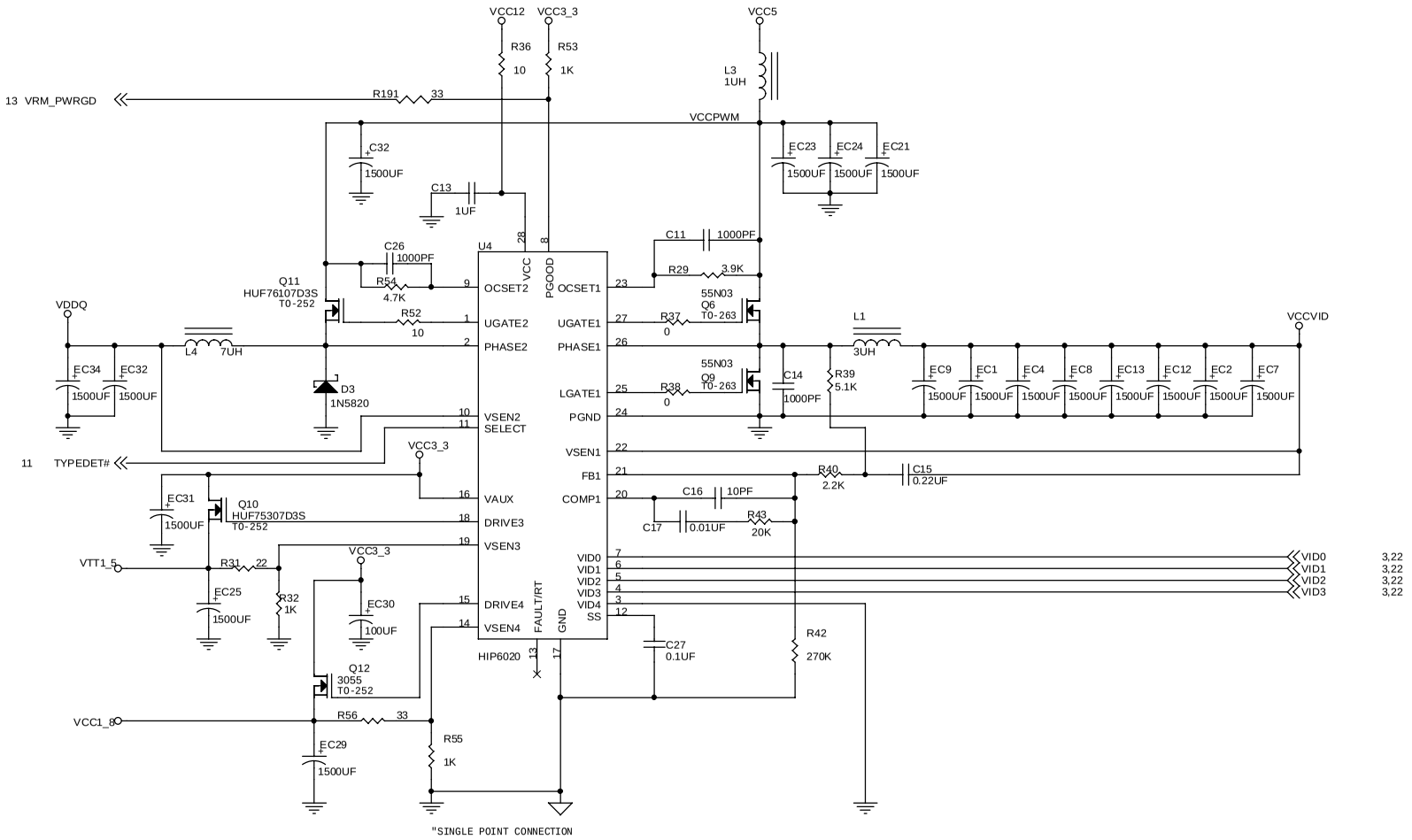

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Title: VOLTAGE REGULATORS PART 1		
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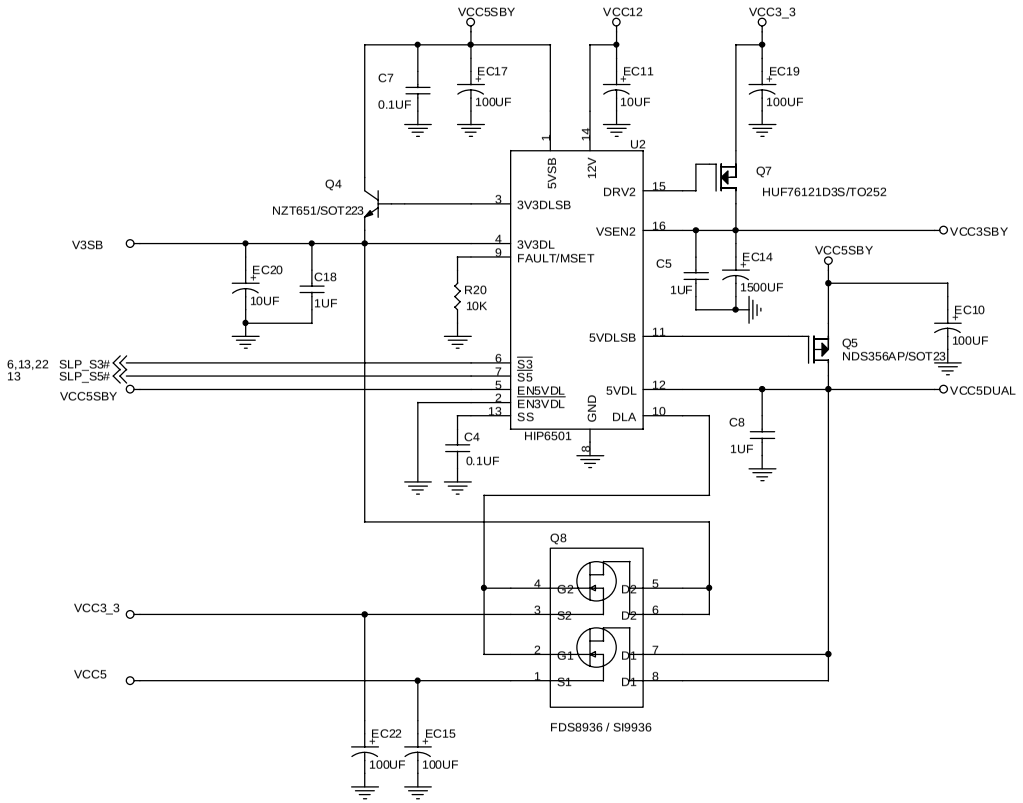

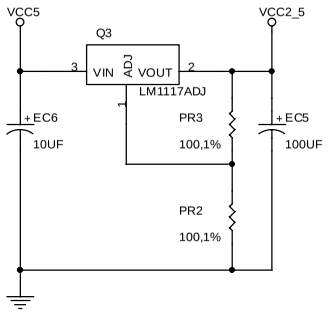

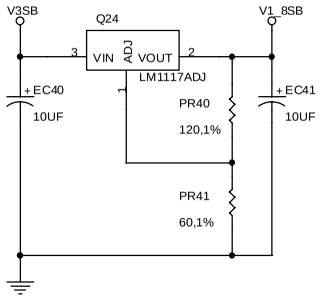

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ABIT Computer Corp.

Title	VOLTAGE REGULATORS PART 2	
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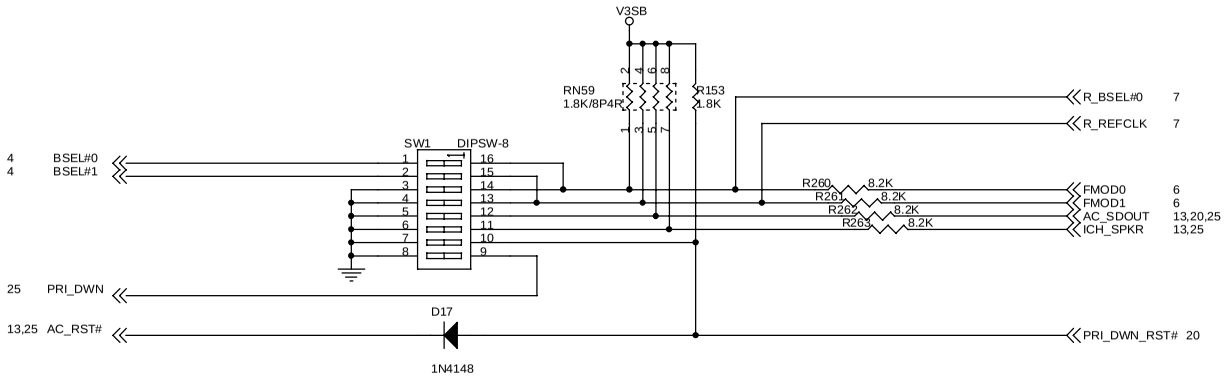

SW2:7-8	ON BOARD AC97 CODEC
ON 7	PRIMARY CODEC
ON 8	DISABLE

SW2:1-2	FSB / SYSTEM MEMORY
ON1-2	CPU DEFAULT
OFF 1-2	BY SW2:3-4

SW2:3-4	FSB / SYSTEM MEMORY
ON ON	66M/PC100
OFF ON	100M/PC100
OFF OFF	133M/PC100 OR PC133

SW2:5	AC_SDOUT
ON	USE CPU FREQ STRAP IN ICH REGISTER
OFF	FORCE CPU FREQ STRAP TO SAFE MODE(1111)

SW2:6	STRAP(SPKR)
ON	NO REBOOT ON 2ND WATCHDOG TIMEOUT
OFF	REBOOT ON 2ND WATCHDOG TIMEOUT

ABIT Computer Corp.

Title: SYSTEM CONFIGURATION

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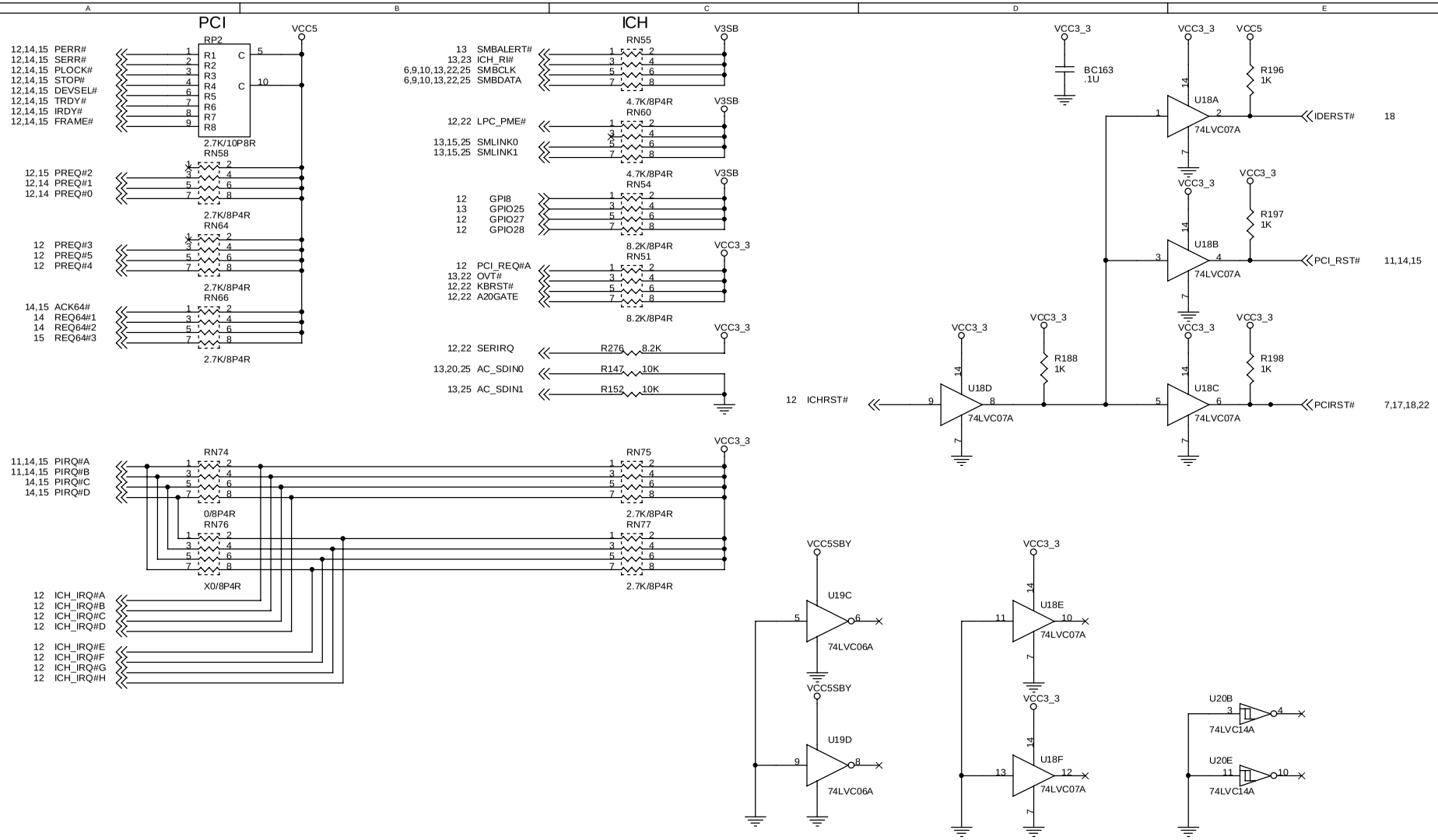

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Title	PU/PDR & UNUSED GATES	
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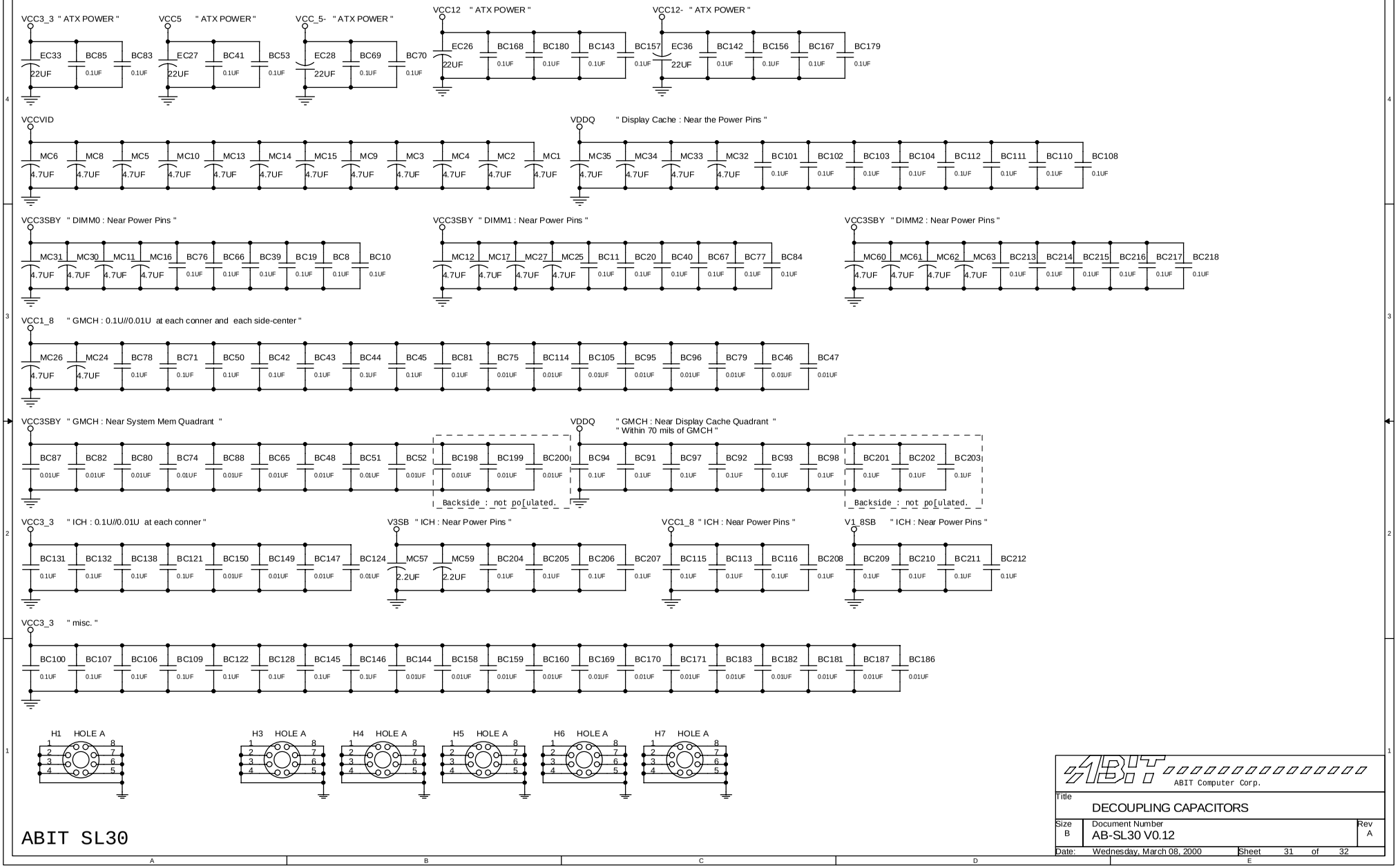
VCC3_3 " ATX POWER "
EC33 22UF
BC85 0.1UF
BC83 0.1UF
VCC5 " ATX POWER "
EC27 22UF
BC41 0.1UF
BC53 0.1UF
VCC_5- " ATX POWER "
EC28 22UF
BC69 0.1UF
BC70 0.1UF
VCC12 " ATX POWER "
EC26 22UF
BC168 BC180 BC143 0.1UF
BC157 0.1UF
VCC12- " ATX POWER "
EC36 22UF
BC142 BC156 BC167 BC179 0.1UF
VCCVID
MC6 MC8 MC5 MC10 MC13 MC14 MC15 MC9 MC3 MC4 MC2 MC1 4.7UF
VDDQ " Display Cache : Near the Power Pins "
MC35 MC34 MC33 MC32 4.7UF
BC101 BC102 BC103 BC104 BC112 BC111 BC110 BC108 0.1UF
VCC3SBY " DIMM0 : Near Power Pins "
MC31 MC30 MC11 MC16 4.7UF
BC76 BC66 BC39 BC19 BC8 BC10 0.1UF
VCC3SBY " DIMM1 : Near Power Pins "
MC12 MC17 MC27 MC25 4.7UF
BC11 BC20 BC40 BC67 BC77 BC84 0.1UF
VCC3SBY " DIMM2 : Near Power Pins "
MC60 MC61 MC62 MC63 4.7UF
BC213 BC214 BC215 BC216 BC217 BC218 0.1UF
VCC1_8 " GMCH : 0.1U//0.01U at each conner and each side-center "
MC26 MC24 4.7UF
BC78 BC71 BC50 BC42 BC43 BC44 BC45 BC81 BC75 BC114 BC105 BC95 BC96 BC79 BC46 BC47 0.1UF 0.01UF
VCC3SBY " GMCH : Near System Mem Quadrant "
BC87 BC82 BC80 BC74 BC88 BC65 BC48 BC51 BC52 BC198 BC199 BC200 0.01UF
Backside : not po[ulated.
VDDQ " GMCH : Near Display Cache Quadrant "
" Within 70 mils of GMCH "
BC94 BC91 BC97 BC92 BC93 BC98 0.1UF
BC201 BC202 BC203 0.1UF
Backside : not po[ulated.
VCC3_3 " ICH : 0.1U//0.01U at each conner "
BC131 BC132 BC138 BC121 BC150 BC149 BC147 BC124 0.1UF
0.01UF
V3SB " ICH : Near Power Pins "
MC57 MC59 2.2UF
BC204 BC205 BC206 BC207 0.1UF
VCC1_8 " ICH : Near Power Pins "
BC115 BC113 BC116 BC208 0.1UF
V1_8SB " ICH : Near Power Pins "
BC209 BC210 BC211 BC212 0.1UF
VCC3_3 " misc. "
BC100 BC107 BC106 BC109 BC122 BC128 BC145 BC146 BC144 BC158 BC159 BC160 BC169 BC170 BC171 BC183 BC182 BC181 BC187 BC186 0.1UF 0.01UF
H1 HOLE A
H3 HOLE A
H4 HOLE A
H5 HOLE A
H6 HOLE A
H7 HOLE A

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ABIT Computer Corp.

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